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LECTRONIC DESIGN

14 IIII 94

MAY 2, 1994

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

MOSFET HIP BREAKS N-RESISTANCE OLTAGE BARRIER

ANALOG PROCESSES CHALLENGE DESIGNERS

TECHNOLOGY ANALYSIS: CICC REVIEW

ELECTRO PREVIEW

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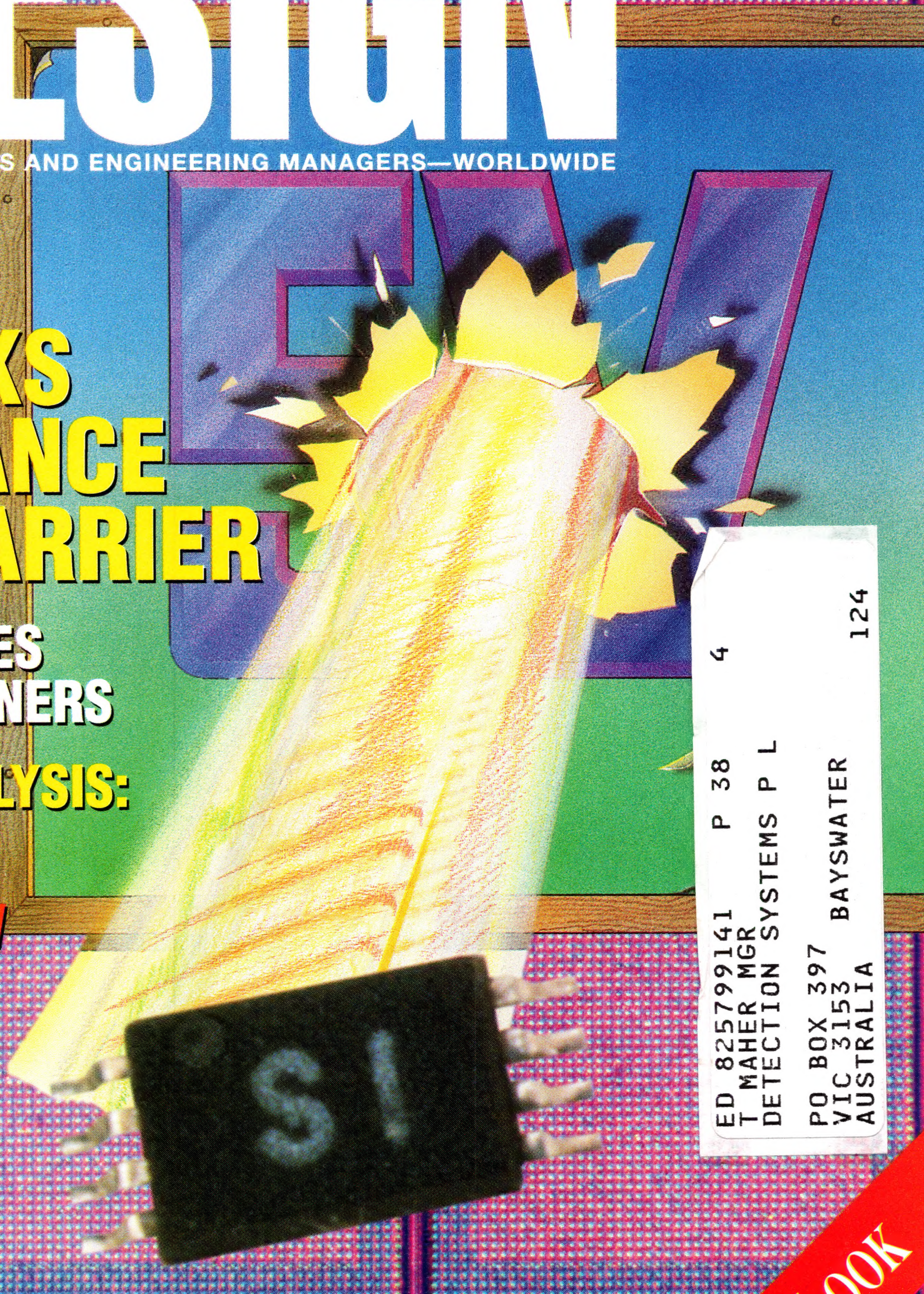

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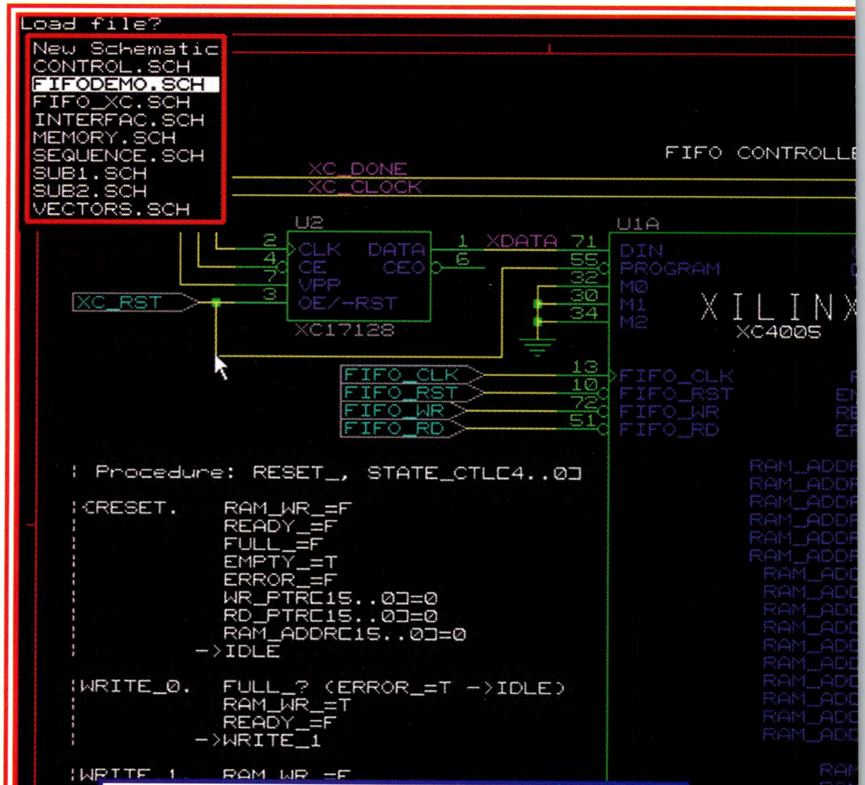
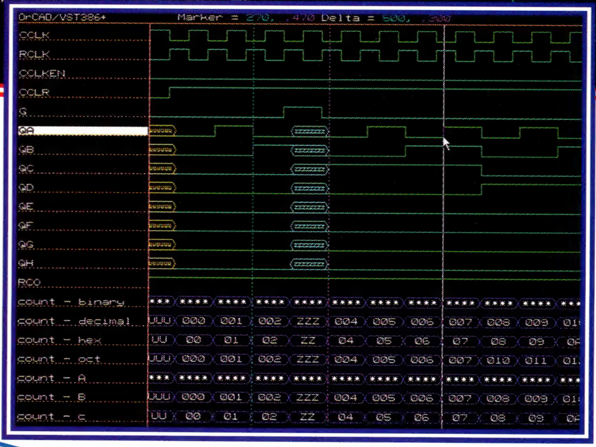
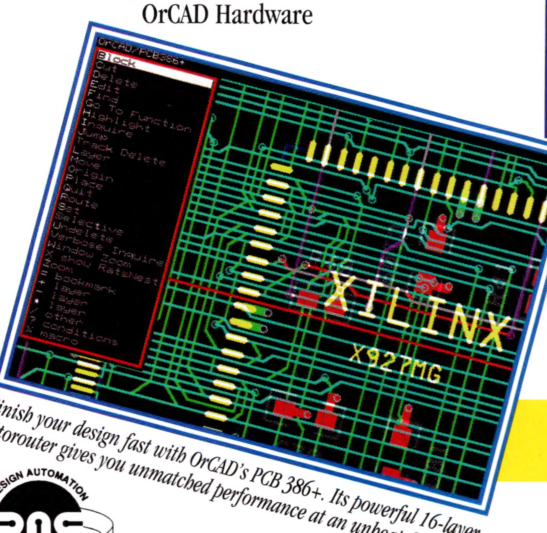


```
! Procedure: RESET_, STATE_CTL[4..0]
!<RESET.     RAM_WR_=F
!            READY_=F
!            FULL_=F
!            EMPTY_=T
!            ERROR_=F
!            WR_PTR[15..0]=0
!            RD_PTR[15..0]=0
!            RAM_ADDR[15..0]=0
!          ->IDLE
!WRITE_0.    FULL_? (ERROR_=T ->IDLE)
!            RAM_WR_=T
!            READY_=F
!          ->WRITE_1
!WRITE_1.    RAM_WR_=F
```



(Top) Combine S 386+ and PLD 38 design your boar and the programm logic devices that populate them. (Left) Design verification is fas easy with VST 386 And, it's supporte Xilinx, Actel, and major FPGA vendo



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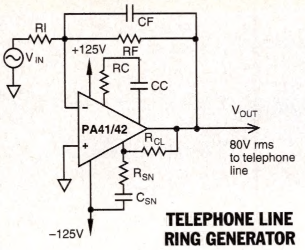

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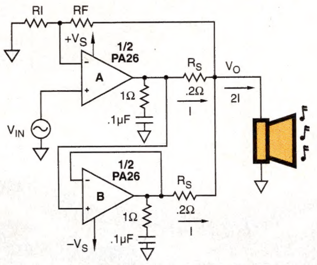
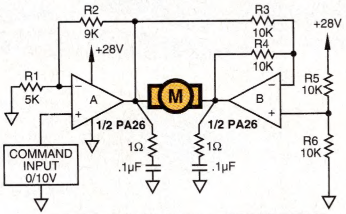


5A AUDIO PARALLEL CONNECTION



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PA42	100V-350V	120mA	$\pm V_S-12V$	10V @ 40mA	SIP[1]	$13.60
PA41M[2]	100V-350V	120mA	$\pm V_S-12V$	10V @ 40mA	TO-3[1]	$46.62

[1] The TO-3 is a hermetic package; the SIP is a non-hermetic package

[2] "M" designates hi-rel military grade

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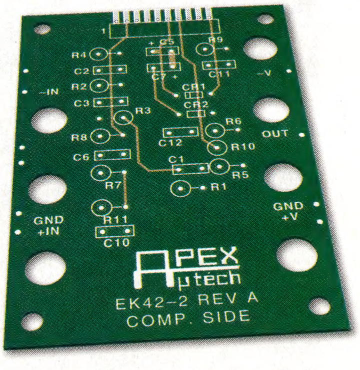

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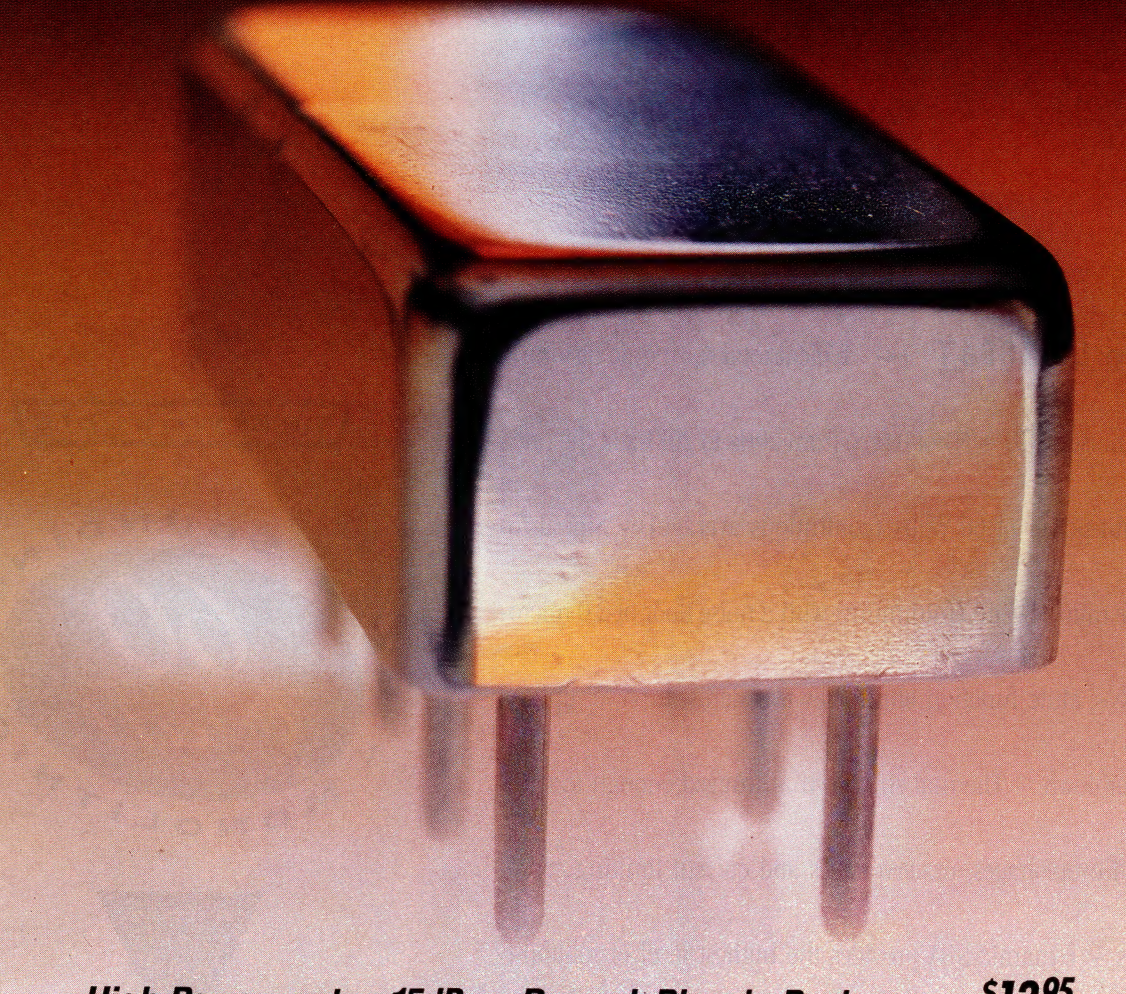

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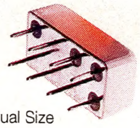
MAN-2	0.5-1000	18	1.5	7.0	6.0	37	12/85	15.95
MAN-1LN	0.5-500	28	1.4	8.0	2.8	42	12/60	15.95
^MAN-1HLN	10-500	10	0.8	15.0	3.7	16	12/70	15.95
MAN-1AD	5-500	16	1.0	6.0	7.2	50	12/85	24.95
MAN-2AD	2-1000	9	0.7	-2.0	6.5	33	15/22	22.50
MAN-11AD	2-2000	8	1.5	-3.5	6.5	27	15/22	29.95

* Midband $10f_L$ to $f_U/2$, +/- 0.5 dB ** At 1dB compression point ^ Case height 0.3 inch



Actual Size

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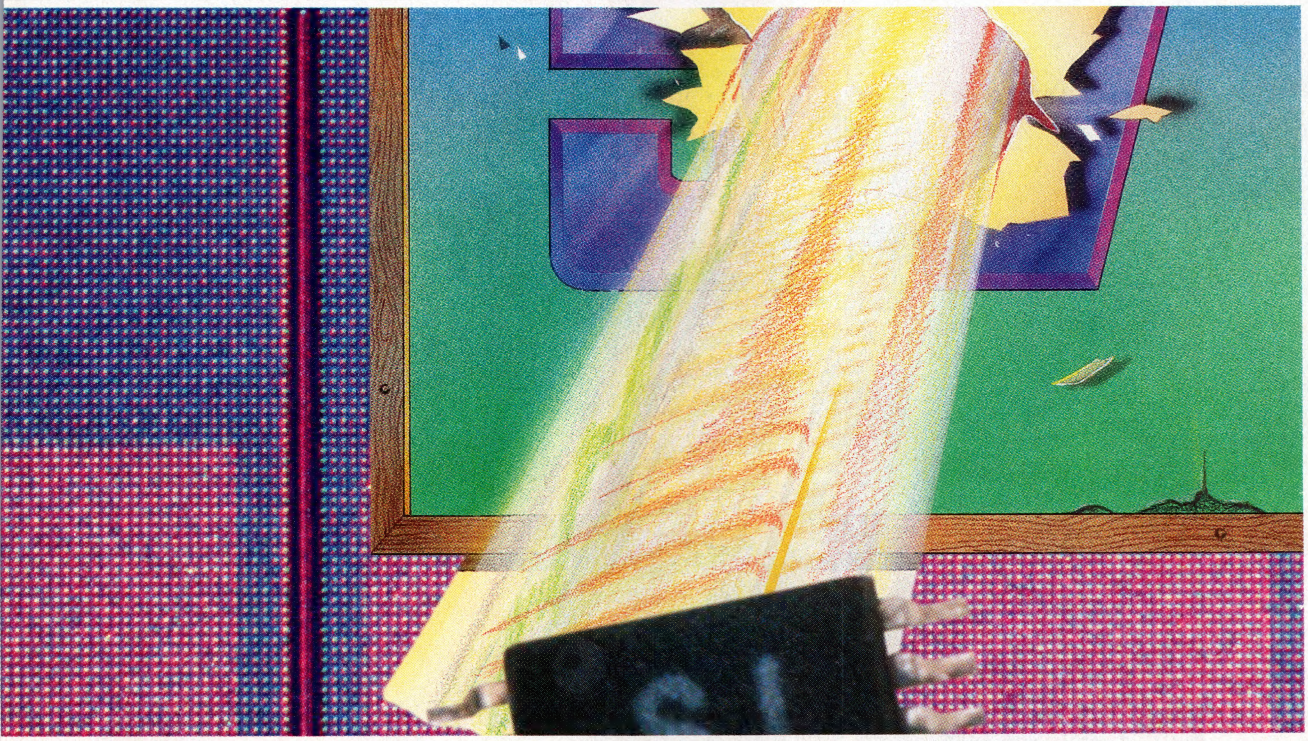

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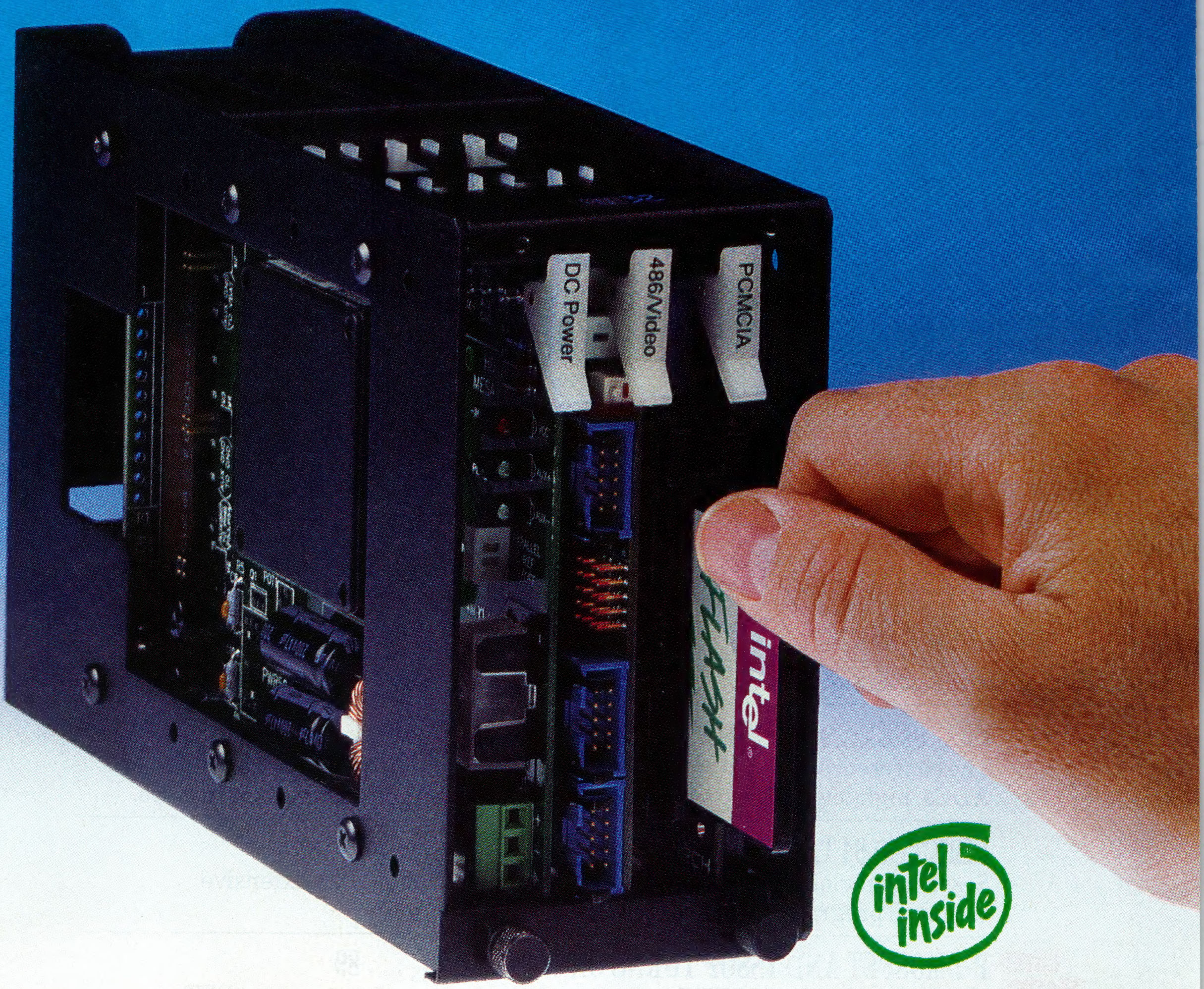
SERIOUS DOWNSIZING



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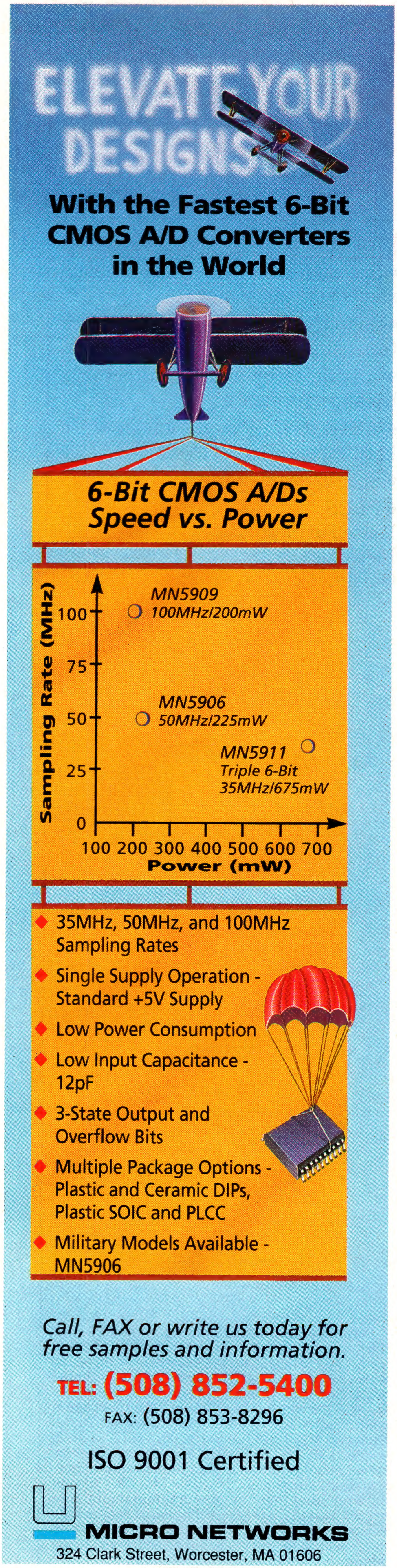

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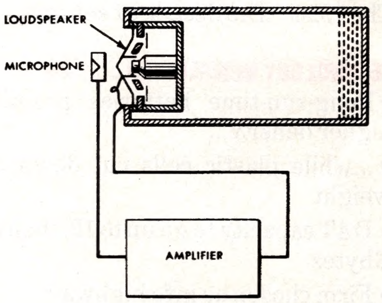

The speaker is mounted directly behind the microphone, as shown. Since the loudspeaker must operate in an enclosed space, a speaker with a cone of only 3-1/2" diameter was designed to keep the enclosure small. The microphone utilizes a subminiature tube called a "mechano-electronic transducer" that contains a rod connecting one element of the tube through the tube enclosure directly to the diaphragm of the microphone. The vibration of the diaphragm by the noise waves is transferred directly to one of the tube elements, thereby developing the signal. The unit was developed by Dr. Harry F. Olson of the RCA Laboratories Division, Radio Corporation of America, Princeton, N.J. The sound absorber can operate on either batteries or house current. *(Electronic Design, May 1954, p. 7.)*

Acoustic cancellation of sound waves has moved far beyond this rudimentary scheme. For example, Noise Cancellation Technologies, Stamford, Conn., is producing noise-reduction products based on digital-signal-processing techniques (see our Nov. 11, 1993 issue, p. 25) for application in quieting aircraft cabins and in consumer items, such as noise-cancelling headsets.—SS

Tubes Replaced Needlessly

A survey of 80,000 tubes rejected by technicians maintaining military equipment revealed that approximately 25% had no defects when tested on a tube tester. This figure indicates poor training of these technicians, according to a paper ("The Effect of Maintenance on Reliability of Complex Military Electronic Equipment") by J.B. Arnold of Aeronautical Radio, Inc., Washington D.C., presented at the recent IRE Convention in New York.

The unnecessarily high replacement rate was ascribed to two factors. First, because of the complexity of some present military equipment, technicians resort to wholesale tube replacement to remedy failures. The replacement may only mask the real trouble, so that tubes soon fail and the equipment is again out of service. Secondly, maintenance procedures often call for testing large numbers of tubes periodically or as a means of trouble-shooting. Continual removal of tubes from their sockets can damage many tubes. In addition, reliance is placed on the tube checker to determine whether the tube will operate in the circuit, when, actually, performance in the circuit itself should be the criterion. To correct this wasteful situation, Mr. Arnold urged that the gap between equipment complexity and the educational level of the technician be narrowed. *(Electronic Design, May 1954, p. 10.)*

The more things change, the more they remain the same. This problem of constant rejection and replacement reemerged with the arrival of the computer board: Many service technicians simply swapped boards until the equipment worked again, and then shipped the lot of boards—good and bad—back to the repair depot, where they became someone else's problem.—SS

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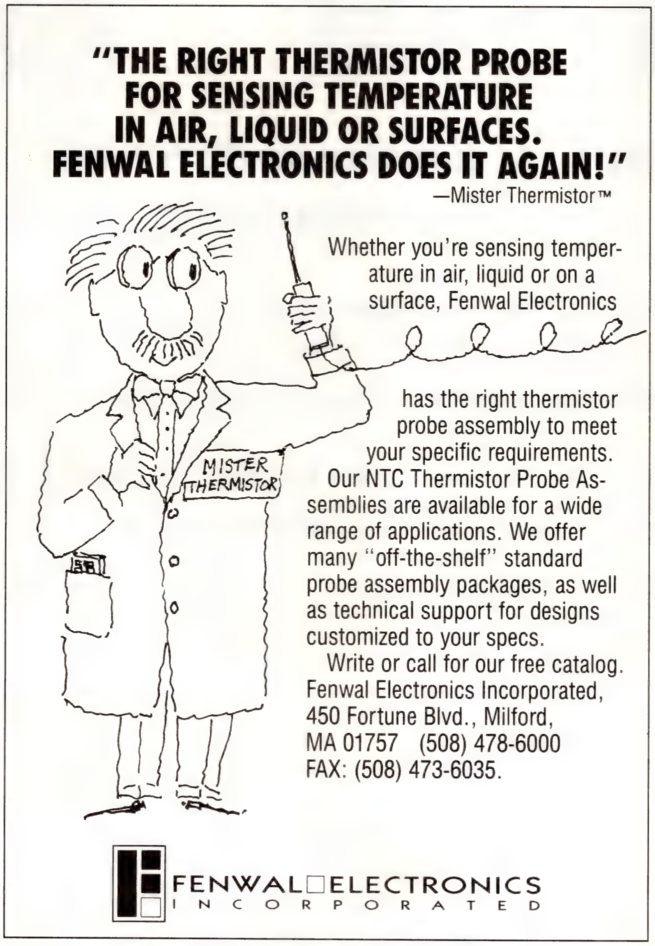
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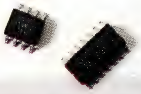

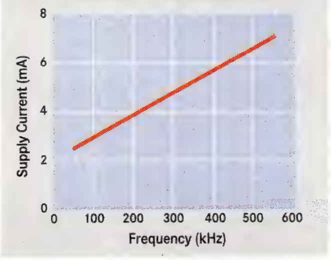

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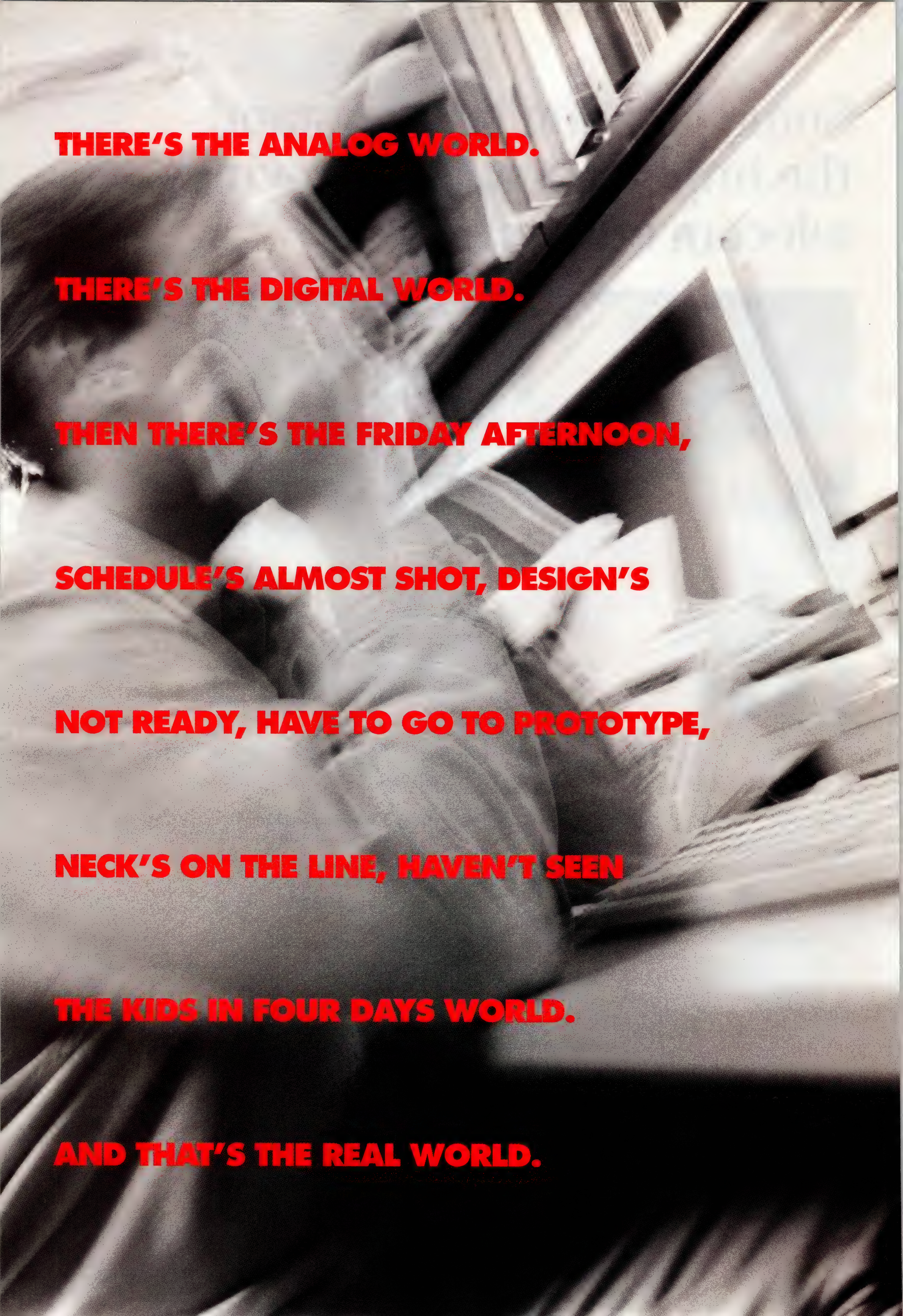
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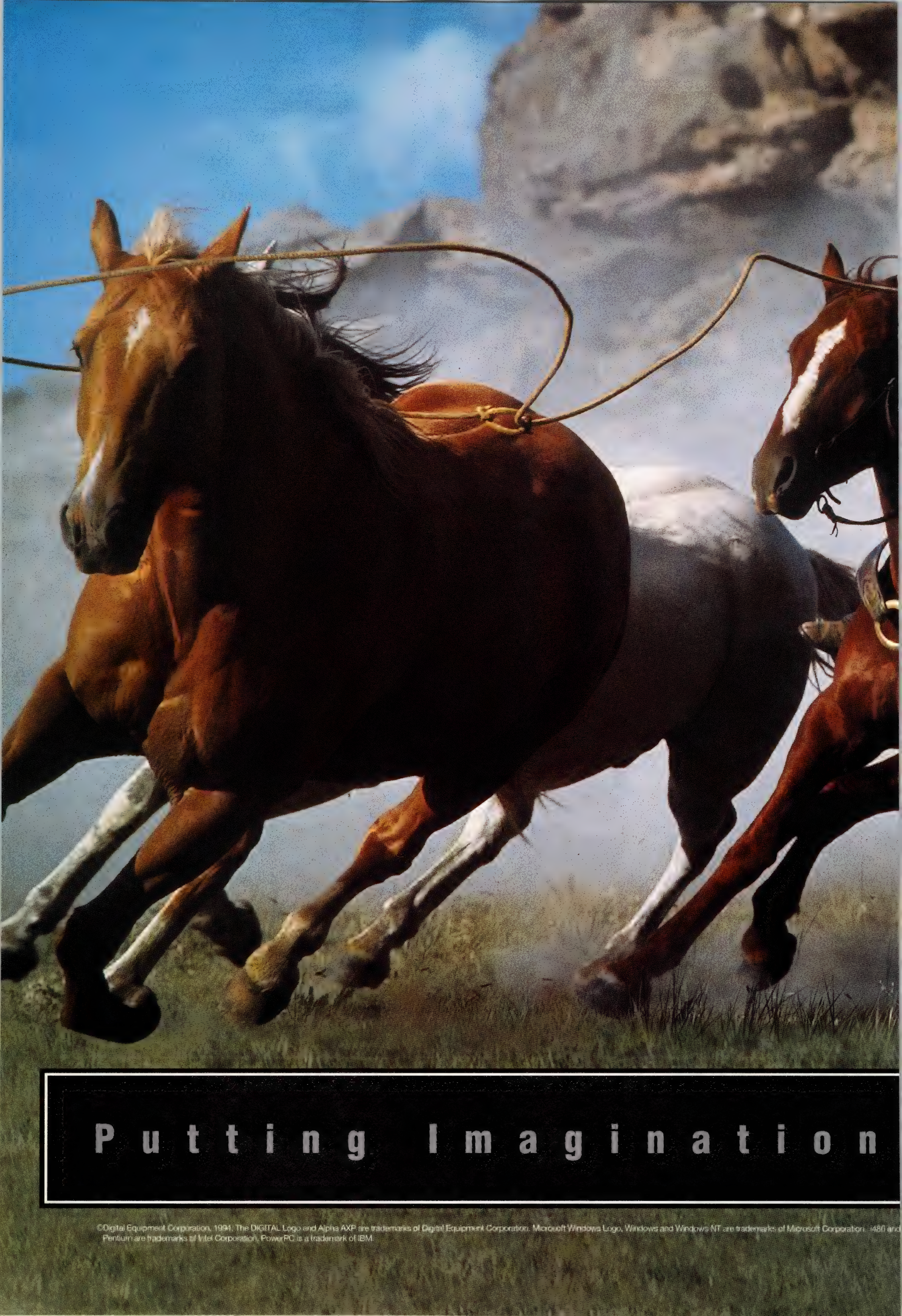

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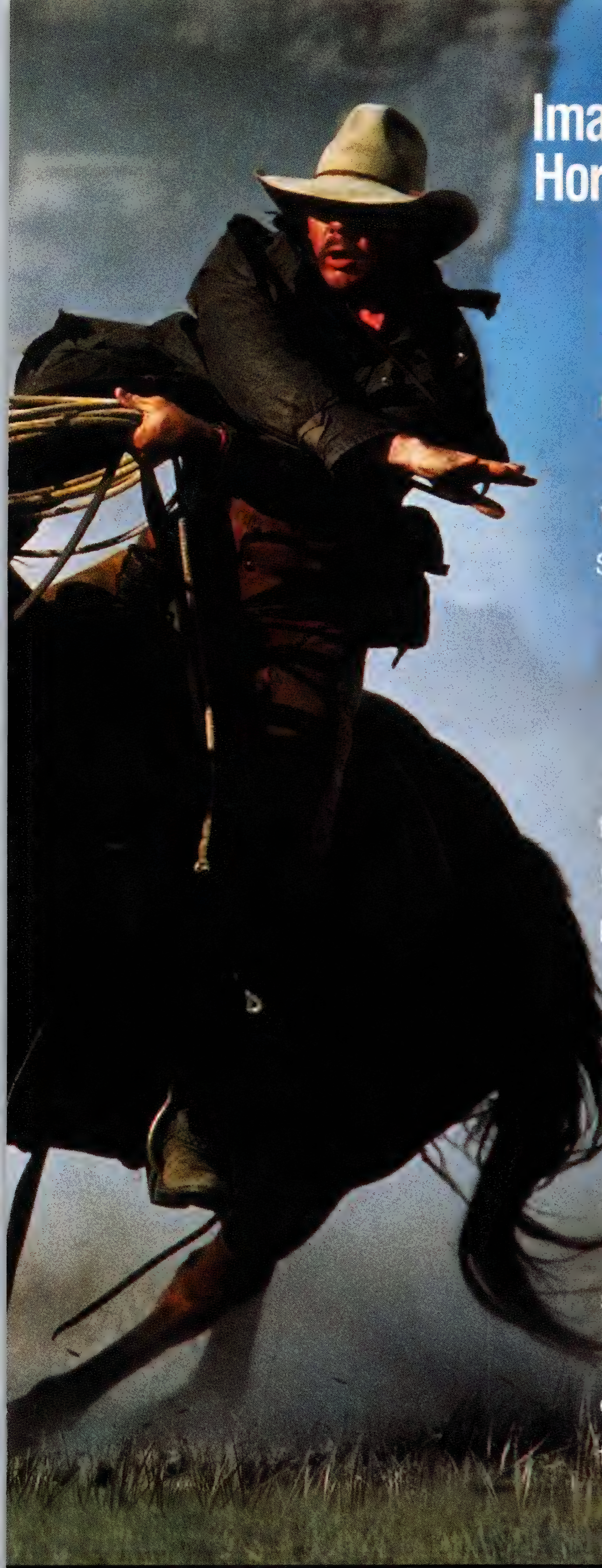

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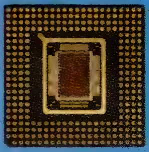

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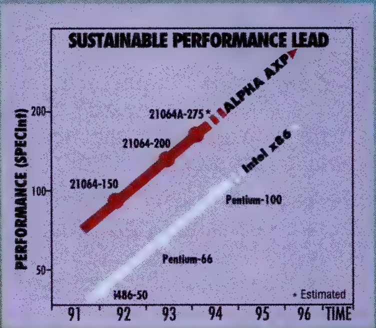

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PARADIGM SHUFFLE

It's a little bit like an earthquake. We all know it's going to happen, we just don't know exactly when. It's a landmark event. In the world of technology, it has come to be called a paradigm shift. We in the news media have been writing for several years now about the challenges of deep submicron geometries. Much of the verbiage has been about the processes themselves. It was thought that once the processes were tweaked to perfection, an era of fast, small, and inexpensive ASICs would follow.

What's actually happening at the "bleeding edge" is often quite different. Designs consuming four times the power that was forecast is one ugly outcome. Sometimes the designs don't work. That's worse.

The problem is that designing deep submicron devices is an even greater challenge than developing the process technology.

You've heard it all before: as feature sizes shrink, design complexity increases because more functions can be integrated into the same die area. Parasitics become more important considerations for timing. Predicting power consumption is like rolling dice.

Over the past several weeks, I've talked to a few people who believe that simulation methodologies based on gate-level simulation may not be able to deal effectively with deep submicron designs.

I'm not sure about that. Clever people will come up with ingenious solutions, and we should recall that successful technologies are always a moving target. They get better and better at doing what they could not do last year.

The disk-drive industry is a great example of this pattern. Magnetic-drive makers have been extremely successful at improving their price-performance ratio to keep the solid-disk companies and optical-drive makers at bay.

On the other hand, I have considerable difficulty imagining how gate-based methodologies can handle the nonlinearities that are so prominent in deep submicron designs, and how they can reliably predict power consumption. Gates are, after all, a figment of our imagination. We like to think in terms of OR and NOR. Gates don't exist on silicon. Transistors do.

Some leading-edge companies are already looking at a chip as if it were a micro-pc board, populating the silicon with modules that communicate with each other. With that in mind, I'm wondering if we're in for a paradigm shift in ASIC simulation. Let me know what you think.

Josh Shandle

Editor-in-Chief

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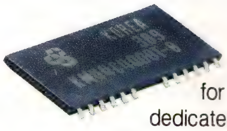

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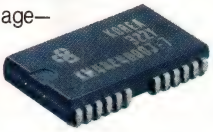
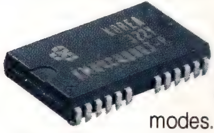


Samsung's 16M DRAMs have been optimally designed in x1/x4 and x8/x16 chip sets with fast access times of 50/60/70ns. A new extended data output(EDO)mode enhances access times over chips that use conventional fast page modes. Moreover, these chips are extremely energy efficient, drawing not 5volts, but a mere 3.3volts of power.



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4MX 4	Fast Page	KM44C(V) 4000A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4100A/AL/ASL/ALL	2048Cycle/32ms
	Static Column	KM44C(V) 4002A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4102A/AL/ASL/ALL	2048Cycle/32ms
	Quad-$\overline{\text{CAS}}$	KM44C(V) 4003A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4103A/AL/ASL/ALL	2048Cycle/32ms
	EDO (Hyper Page)	KM44C(V) 4004A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4104A/AL/ASL/ALL	2048Cycle/32ms
2MX 8	Fast Page	KM48C(V) 2000A/AL/ASL/ALL	4096Cycle/64ms
		KM48C(V) 2100A/AL/ASL/ALL	2048Cycle/32ms
1MX16	Fast Page	KM416C(V) 1000/L/LL	4096Cycle/64ms
		KM416C 1200/L/LL	1024Cycle/16ms
1MX 4	Fast Page	KM44C(V) 1000C/CL/CSL/CLL	1024Cycle/16ms
	Static Column	KM44C(V) 1000C/CL/CSL/CLL	1024Cycle/16ms
	Quad-$\overline{\text{CAS}}$	KM44C(V) 1003C/CL/CSL/CLL	1024Cycle/16ms
	EDO (Hyper Page)	KM44C(V) 1004C/CL/CSL/CLL	1024Cycle/16ms
4MX 1	Fast Page	KM41C(V) 4000C/CL/CSL/CLL	1024Cycle/16ms
	Static Column	KM41C(V) 4000C/CL/CSL/CLL	1024Cycle/16ms
	EDO (Hyper Page)	KM41C(V) 4004C/CL/CSL/CLL	1024Cycle/16ms

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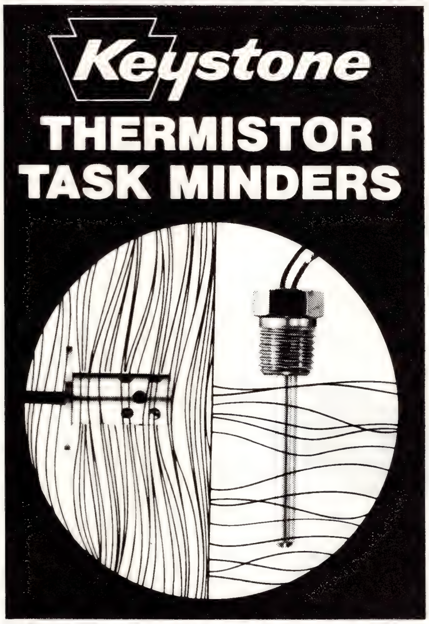

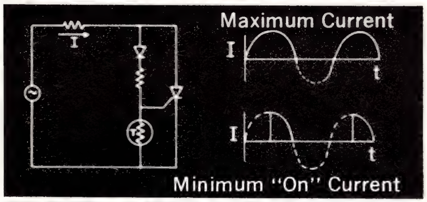

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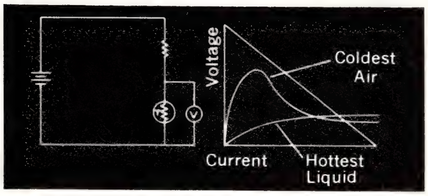

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TECHNOLOGY BRIEFING

THE 1990S: THE DECADE OF SENSORS?

Since their introduction back in the 1950s, sensors and silicon micromachining have reached many significant milestones. Numerous advances in electronics and micro-fabrication technology touched off revolution in the sensor industry.

Today, while sensors are being designed into a wide range of applications researchers are continually looking for ways to make sensors better, and t develop a larger variation of sensor types. Public and private research labs such as the Sandia National Laboratory, the National Institute for Standard and Technology, Lucas NovaSensor, and Analog Devices, are only a few tha have made commitments to aid in the progression of sensor technology.

In the upcoming years, I expect that we will have many things to look forwar to. The sensor market is moving toward a higher level of integration an performance. Trends in on-chip capabilities include offset balance, temperatur compensation, signal normalization, signal amplification, and temperatur sensing. But these are only the beginning. Another developing trend, judging by several recent announcements, is the shrinking size of sensors.

CHERYL J. AJLUNI
WEST COAST EDITOR

One such example is a hydrogen sensor, developed at the Sandia National Laboratory, which offers reliable detection of hydrogen. It's smaller (0.0004 liter), faster, sturdier, and less expensive to manufacture (thanks to standard microelectronics technology) than other existing techniques to detect hydrogen. With detection capability over a range of 0.0001% to 100%, and performance reliability in the temperature range of –100°C to 140°C, it can be used in extreme-environment applications, such as leak detection during space-shuttle launches, and detecting transformer failure in electric power plants.

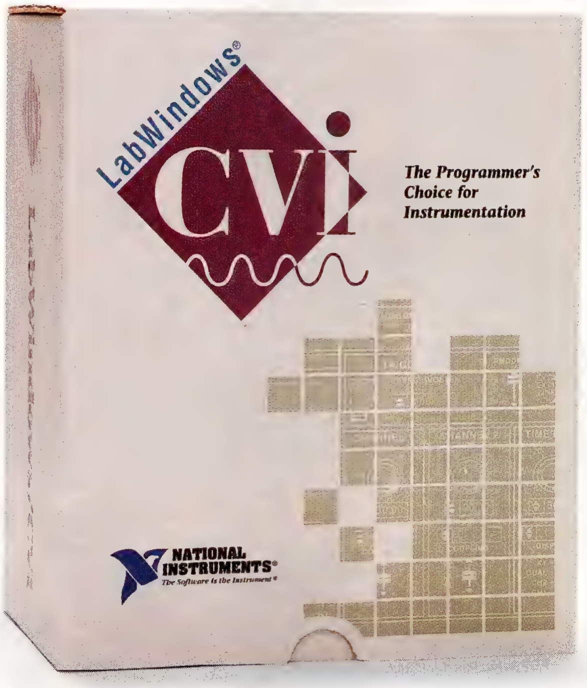
Another big player in the sensor industry, Lucas NovaSensor, recentl introduced a smart pressure transducer. The transducer offers a compensate high-level output signal in addition to a 1% interchangeable calibration over th temperature range –20°C to 85°C. Developed as a high-performance, low-cos option for OEM applications like industrial instrumentation and test, th transducer is the first of its kind to offer digital signal processing. Moreove its programmable design allows for easy customization of various parameters including scaling and offset.

Also on the horizon is a set of interface standards that's based on existin sensor technologies, yet flexible enough to accommodate future technologies While these standards may be a few years off, their eventual acceptance wil have a widespread impact on the sensor community.

These standards will establish a general communication protocol and dat format. They also will select standard connectors for smart sensors an transducers, and several hardware implementations, as well as establish public domain library of software drivers for them. Standards will guarantee in essence, that sensors can interface with one another and invariably simplif their application and integration. In addition, they will provide a better understanding of emerging sensor technology and help to expand the use of sensor in many manufacturing and other types of systems.

Obviously, these trends and emerging standards will significantly affect th sensor industry as it stands today. Sensors will become more widely available t many different industries, from automotive to aerospace. In the automotive industry alone, the estimated growth rate is 30% per year. As the industry continues t expand in this field, we will start to see the impact on the way we live and work Smarter sensors will mean everyday tasks become simpler. For instance, adjustin your office temperature or checking the pressure in your car tires will no longe be concerns. Many changes lie ahead—expect to see them coming your way soon

Building Permit.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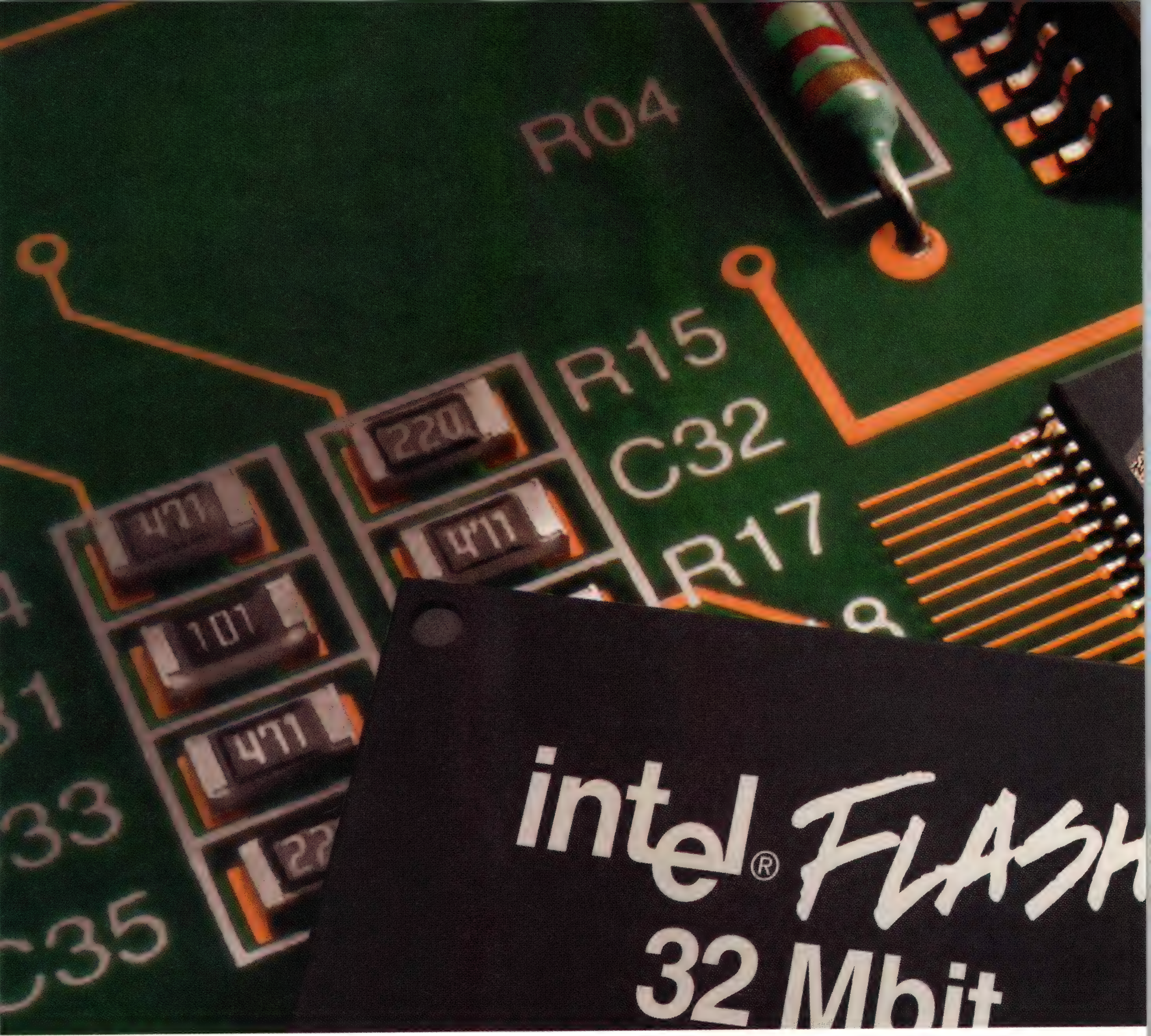

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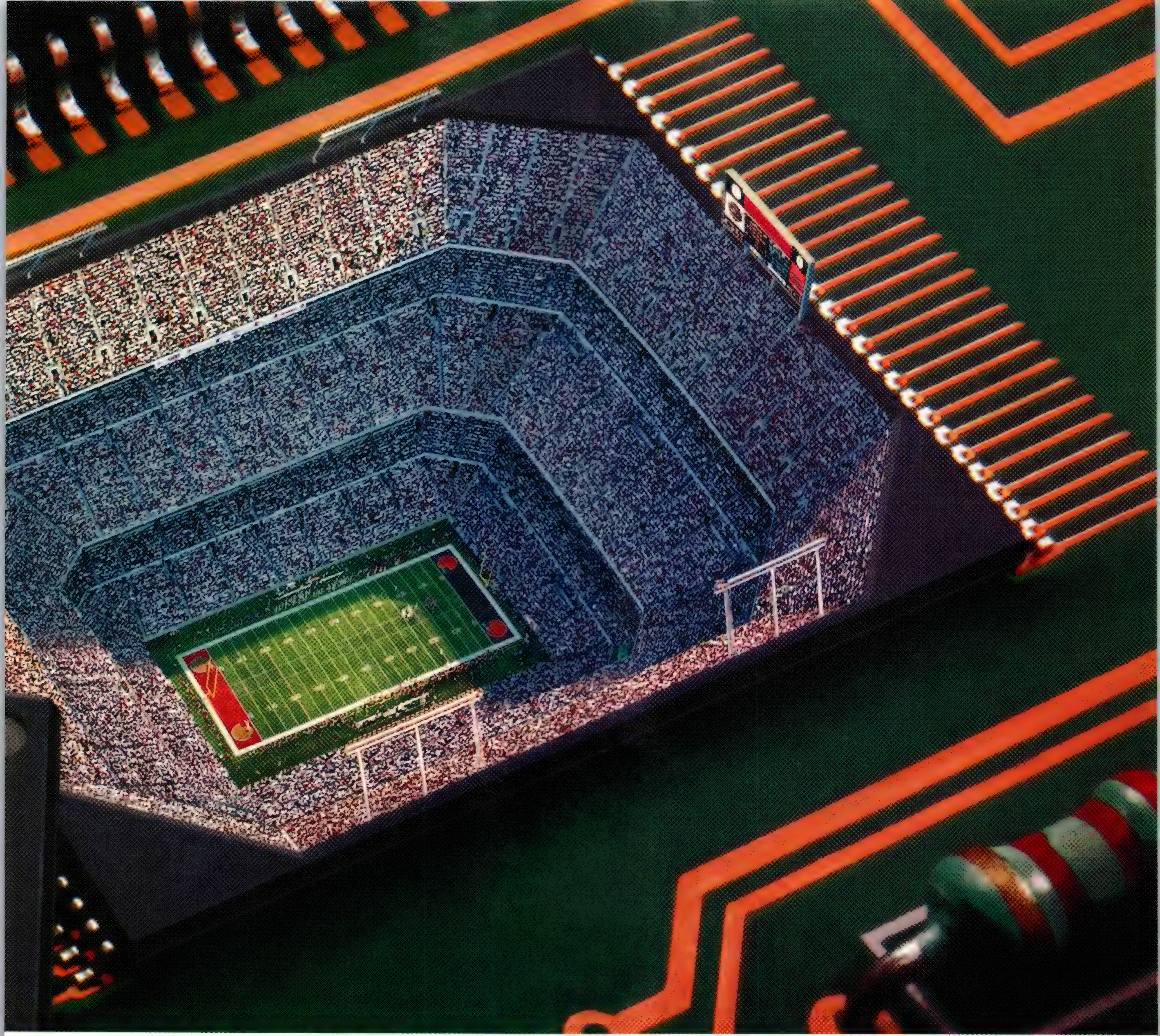

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And when it comes to flash value, Intel is in a eague all by itself. In fact, the 16Mb FlashFile component is the most cost-effective 3.3V flash memory available.

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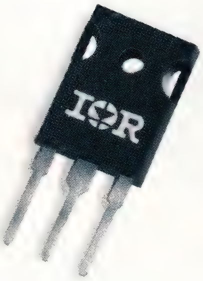
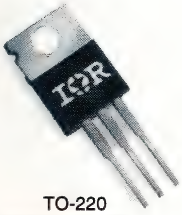
Motor control savings.

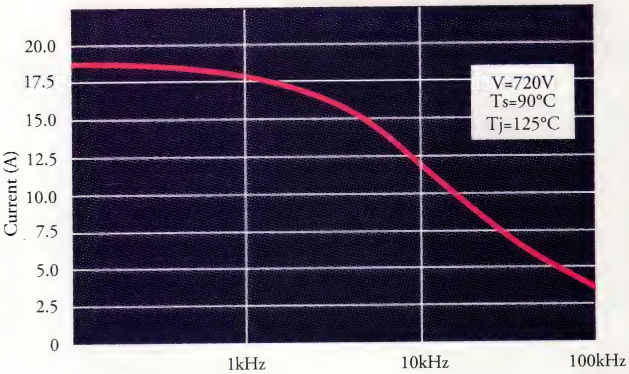
Or how to design noise-free inverters that switch faster for less money. The 1200V IGBT *CoPack*.



TO-247
UltraFast IGBT



TO-220
UltraFast IGBT



Output current vs frequency for two IRGPH50U in half-bridge, 50% duty cycle.

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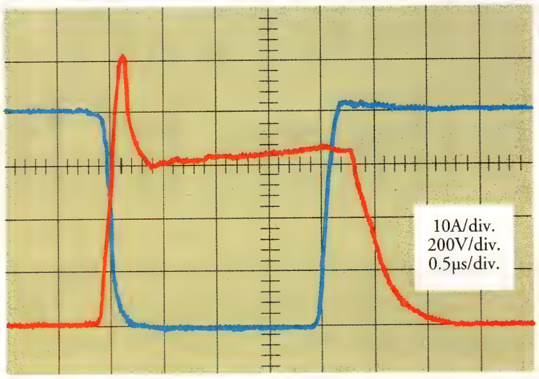

Switching waveforms of the IRGPH50U in a clamped inductive load at Tj=90°C.

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READER SERVICE 92

TECHNOLOGY NEWSLETTER

LONG-RUN-TIME BATTERIES PROMISE HIGHER DENSITY...

The milestone of day-long operation for battery-powered PCs is the goal of a joint development project. Battery maker AER Energy Resources Inc., Atlanta, Ga., and PC developer Zenith Data Systems, Buffalo Grove, Ill. are teaming up to create a long-run-time version of AER Energy's rechargeable zinc-air battery system. It promises from two to four times the energy density by weight of nickel-cadmium and nickel-metal-hydride cells. Depending on the user's work pattern and the computer's configuration and power requirements, AER Energy claims that their system can power a notebook PC for 10 to 20 hours on a single charge. It's hoped that the system can put an end to the trade-offs between a portable computer's feature set and its potential run-time that have plagued system designers since the industry's inception. Contact AER Energy's Frank Harris at (404) 433-2127. *DM*

...WHILE PLASTIC CELLS CUT DOWN ON WEIGHT

Researchers at Bellcore, Livingston, N.J., succeeded in creating a prototype of a flexible plastic, lightweight, high-energy battery that's also rechargeable. Based on lithium-ion technology, the system is more environmentally friendly than traditional liquid rechargeable batteries, such as nickel-cadmium or lead-acid types. It's also capable of equal or better performance at half the weight. The technological breakthrough underlying the prototype is the composition and performance of the polymer matrix. The 3.8-V cells can be cycled several hundred times with less capacity fall-off than their liquid counterparts, and they offer much higher energy density. Their flexible form suits them for thin, flat-cell configurations. They're also leakproof and contain no toxic metals. Originally developed to meet backup power demands for future telecommunication systems, the batteries have myriad potential applications in consumer electronics ranging from pagers, portable PCs, and handheld toys and games to cellular telephones. Contact Cynthia Lucenius at (201) 740-6468. *DM*

DAT CAPACITY TO GO UP TO 12, THEN 24 GBYTES

The Digital Data Storage (DDS) Manufacturers Group recently announced an enhancement to its format-migration path for digital-audio-tape (DAT) storage. The enhancement supplies a 50% capacity increase over current (DDS-3) specifications, which will take the capacity to 12 Gbytes in the native mode and to 24 Gbytes with compression. The DDS-3 format specified 8 Gbytes on a 120-m tape; the 12-Gbyte specification employs 125-m tape. The follow-on specification (DDS-4), which should spawn products by 1997, pushes the capacity to 24 Gbytes. Jumping from 8 to 12 Gbytes will be made possible by refining the head-tape interface and by employing partial-response, maximum-likelihood (PRML) techniques, similar to those used in hard-disk drives. This will increase the number of bits/inch on the tape. The DDS-4 format also will also incorporate the PRML routine, but with thinner tracks on a 180-m tape. Current DDS products top out at a transfer rate of 750-kbytes/. The DDS-3 specification calls for a maximum transfer rate of 1.5 Mbytes/s, while the DDS-4 specification increases the transfer rate to 3 Mbytes/s. Products based on the DDS-3 specification should become available in the second half of the year. For more information, call Hewlett-Packard Co., a member of the DDS Manufacturers Group, at (408) 286-2611. *RN*

FIRM CHOSEN AS INFO HIGHWAY SUPPLIER

Groundwork is being laid for the information highway with help from Sun Microsystems, Mountain View, Calif. The company was chosen by Pacific Bell's California Research and Educational Network as a hardware supplier for four pilot projects. The purpose of the program is to create and test high-speed networked applications that could cut costs, increase productivity, and stimulate new markets in such areas as health care, education, research, and publishing. The four projects are: the Regional Biomedical Information System, which will explore electronic publishing, allowing researchers over a wide geographic area to access time-critical information; Health Care Imaging Information, which will explore the use of high-speed networks to collect and share still and video medical-data images between a hospital and a doctor's office; Tele-education, which employs interactive multimedia over high-speed networks covering long distances; and the Neuro-Imaging Test-Bed Network, which links several hospitals, letting doctors quickly and easily share high-resolution neurological images and associated medical data. Call Sun Microsystems at (415) 336-4690. *RN*

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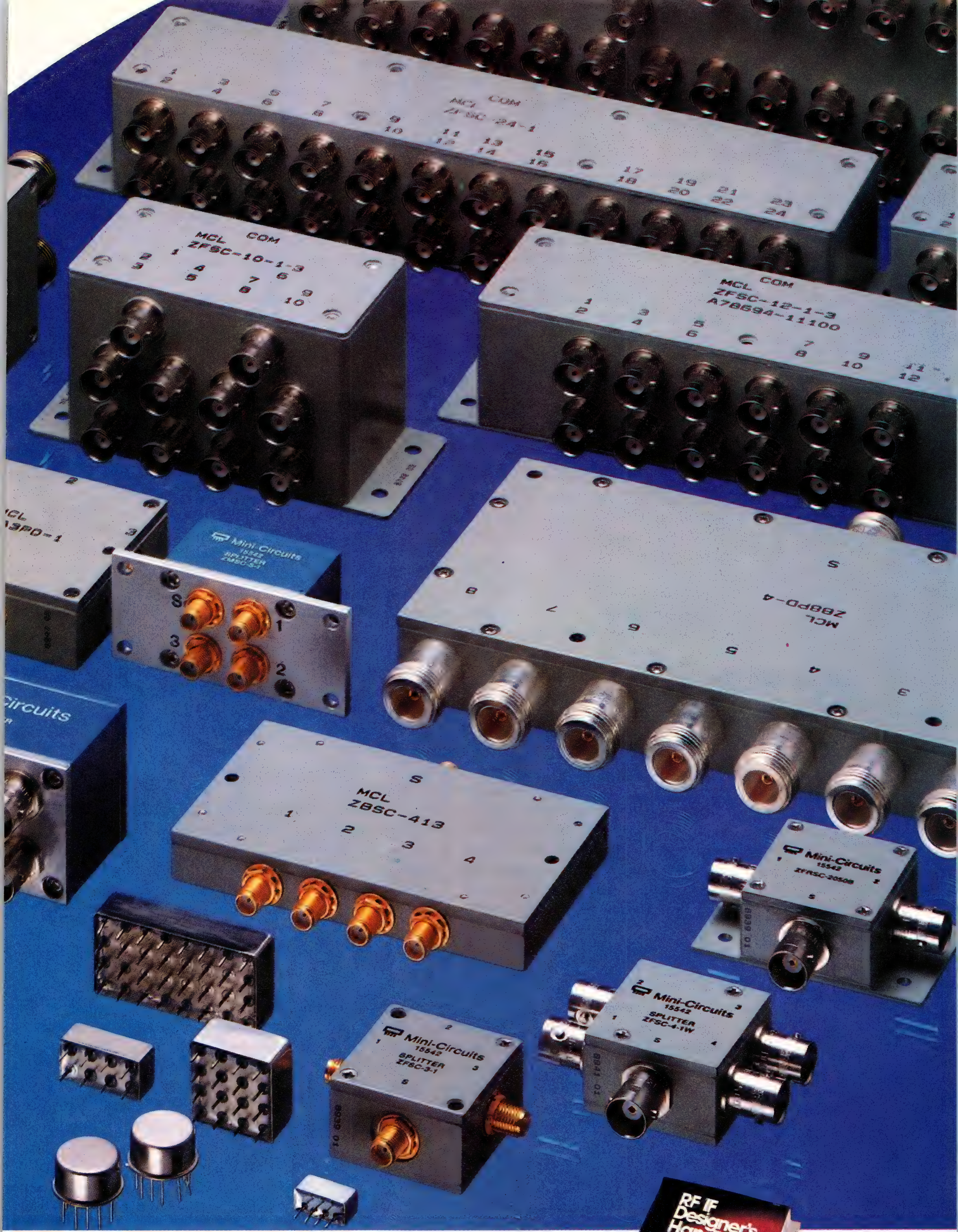
MCL COM ZFSC-24-1
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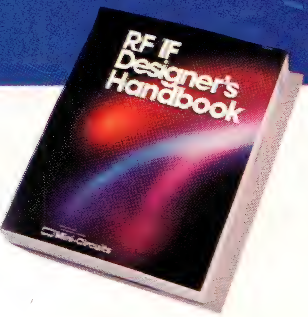


For detailed specs on all Mini-Circuits products refer to
• THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCT DIRECTORY
• EEM • MINI-CIRCUITS' 740-pg HANDBOOK.

READER SERVICE 103

F134 Rev D

SYSTEM REDUCES 3D PROTOTYPING TIME

Researchers at IBM's T.J. Watson Research Center unveiled a rapid prototyping system (RPS) that can create 3D models in a matter of hours without the aid of a technician. The fully automated technology, which can sit on a desktop, frees users from intense production-process training. The system uses CAD or scanned-data computerized-axial tomography (CAT) to create the physical models and parts. However, according to the researchers, the RPS can produce parts from safe, non-toxic plastic or a rubber-like material. The system is based on two computing platforms—a Unix-based RISC System/6000 to run the primary interface and a DOS-based PS/2 Valuepoint to receive the process information and feed it to the printer. Suitable for producing concept models, design-verification models, or patterns for creating molds to produce functional prototypes, the system lets users examine and test models prior to product development. For example, in concept-visualization models, the RPS lets designers detect flaws that are imperceptible on a screen or photo. It also can create molds for short-run manufacturing. Call IBM at (914) 784-6025. *RN*

VGA DISPLAY FITS ON HALF-INCH SQUARE

A newly developed VGA-quality (640-by-480-pixel) active-matrix LCD (AMLCD) imaging device on a 0.5-by-0.5-in. chip delivers a resolution of about 1100 lines/in. With a frame rate of 60 Hz, the Smart Slide chip allows full video-speed connection to all types of personal computers. The chip was developed by the Kopin Corp., Taunton, Mass., and MIT's Lincoln Laboratory under a cooperative R&D agreement signed last fall. Smart Slide, which is based on Kopin's single-crystal silicon technology, has approximately 300,000 transistors in about a 0.25-in.^{2} active area. Control electronics are monolithically integrated with the display. Kopin claims the devices are the smallest, fastest, and densest AMLCD VGA displays. The company says the way it forms the device substantially improves display quality and manufacturability, because ICs can be fabricated first on thin-film, single-crystal silicon using standard IC processing, and then be transferred onto glass. Contact Kopin at (508) 824-6696. *JN*

ARPA WORKS TO CREATE PRACTICAL MCM TOOLS

The Advanced Research Projects Agency (ARPA) recently awarded a two-year contract to Tanner Research Inc., Pasadena, Calif., for the development of affordable, easy-to-use multichip-module (MCM) design tools. The award, funded by ARPA's Application Specific Electronic Module (ASEM) initiative, calls for the company to develop place-and-route, signal-integrity, design-partitioning, packaging, testability, and thermal-analysis software. A major goal of the project is to attain unprecedented integration and ease of use, which hopefully will ensure that MCM technology becomes as accessible to system designers as ASIC technology is today. Under the ASEM program, ARPA awarded contracts to MCM fabricators to reduce product cost and turnaround time. However, the Tanner Research project is directed at eliminating the MCM accessibility barrier created by the high price of existing design tools. Tanner is working closely with MCM designers, fabricators, and industry organizations to specify and test software features and interfaces to streamline design. Call Tanner Research at (818) 792-3000. *LM*

ON-LINE DATA SERVICE EXPANDS SOURCE LIST

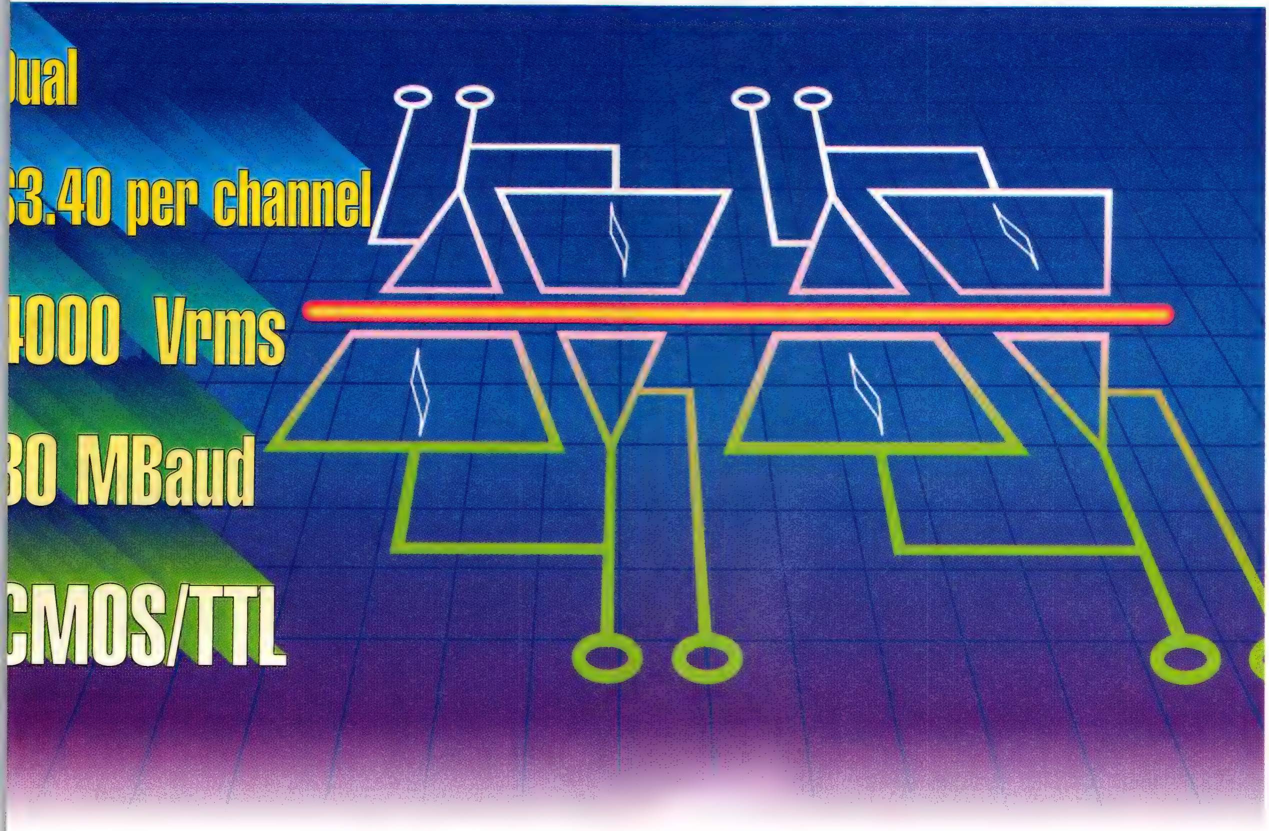
Thirty manufacturers have been added to the list of vendors that contribute information to the EnGenius on-line data service from Info Enterprises Inc., Chandler, Ariz. The recent additions include Advanced Micro Devices, Cypress Semiconductor, Micron Technology, Philips, and Sharp. EnGenius helps engineers by providing current information on components like microprocessors, microcontrollers, memories, and connectors. Engineers can use their desktop computer and a modem to search for, view, and print up-to-date technical specifications, application notes, errata, and other critical information. Future versions of the on-line service will exploit multimedia capabilities, as well as interactive features that let users ask questions and make requests of vendors. Call Info Enterprises at (800) 851-7536 or (602) 267-4636; e-mail: engenius@info-ent.com. *LM*

EDA DATA-EXCHANGE STANDARD IS READY

The Electronic Industries Association (EIA), Washington D.C., is announcing that version 3 0 0 of the Electronic Design Interchange Format (EDIF) standard is now shipping. EDIF aims to simplify the exchange of data among EDA tools. Developed by both tool vendors and users, it's able to handle schematic frames and structured connectivity information. The EIA also is announcing a site-licensing program. The license is required by any company developing an EDIF interface or creating tools based on the EDIF V3 0 0 syntax and information model. Copies of the standard are available on paper or in electronic format. Call Patti Rusher at (202) 457-4962. *LM*

EW

Isolated Bi-Directional Digital Coupler



er Than Optocouplers

50 was designed to replace optocouplers—it uses high
e capacitors instead of an LED/photodiode combination to
it signals across the isolation barrier. (Optocouplers require
current pulses to drive the LED, causing noise spikes on the
supply line.) Its combination of low power, high speed, and
st solves many design limitations inherent in optocouplers—
eliable and cost effective alternative! And, **ISO150** is very
use—no external components are required.

vative Solution

50 has two, bi-directional channels—each channel can be
ured independently to transmit or receive signals across the
on barrier. It's an ultra high-speed capacitively coupled digital
that delivers high isolation with very low power consumption.
0150 for a variety of applications including digital isolation
D and D/A conversion, multiplexed data transmission,
ter-to-peripheral interfaces, I/O port isolation in instruments,
inversion, and isolated data acquisition systems.

ISO150 Key Specifications

Data rate	80M Baud (typ)
Power consumption per channel	25mW (max)
Isolated rated continuous	1500 Vrms
Isolated partial discharge (tested)	2400Vrms
Isolated highest allowable	4000 Vrms
Creepage distance	16.5mm

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S H A R P

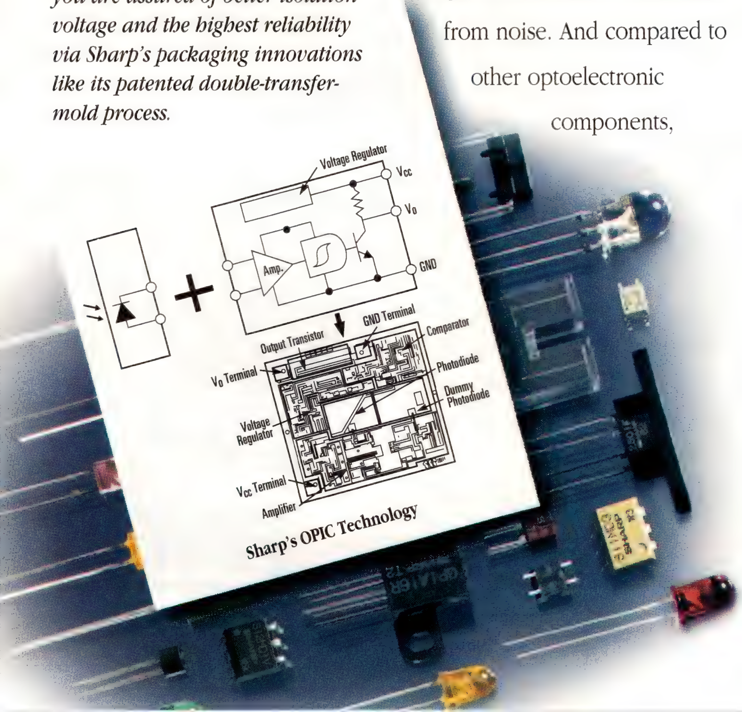
PROGRESS REPORT

Dedicated to the proposition that one good idea leads to another.

No matter how automated, computerized and roboticized tomorrow's production line becomes, its intelligence must be supported by the systems to receive and transmit information and to protect and coordinate its motor skills.

And when you think about everything that goes into an industrial-sized automated system, it's a natural reflex to think of Sharp, the world's leading supplier of both optoelectronic and flat panel display technologies.

With three decades of opto technology behind it, Sharp has pushed device functionality to new extremes. Sharp's proprietary Optical IC (OPIC) process technology combines photodiodes and their peripheral circuitry on a single chip to achieve new dimensions in device miniaturization. In addition, you are assured of better isolation voltage and the highest reliability via Sharp's packaging innovations like its patented double-transfer-mold process.



Sharp's OPIC Technology

GETTING THE LED OUT.

Twenty-five years ago, Sharp introduced the gallium arsenide LED: the heart of the photocouplers and photointerrupters that are the ubiquitous electrical isolators and switching components of industrial control systems.

Sharp photocouplers protect sensitive circuitry from high voltage machines. They give you 1000 times the switching speed of mechanical isolators, plus lower power consumption, smaller size, longer life, and better shielding from noise. And compared to other optoelectronic components,

From early light to the lat

Sharp's opto is well-known for three critical advantages:

**RELIABILITY.
CAPABILITY.
AND CHOICE.**

One faulty photocoupler can be the weak link that paralyzes a production line. Your best hedge against this is the added voltage isolation protection afforded by Sharp's patented double-transfer-mold technology. Sharp uses two separate molds of epoxy resin as

One of Sharp's broad range of CCDs can be the ideal front end of your vision system. Specify high resolution (up to 470,000 pixels) or high sensitivity (up to 600 mV). Choose chips sets, 270,000-pixel color modules, or complete cameras with video output options (composite or Y/C), as well as exposure systems (mechanical or electronic) that can be configured to your needs.

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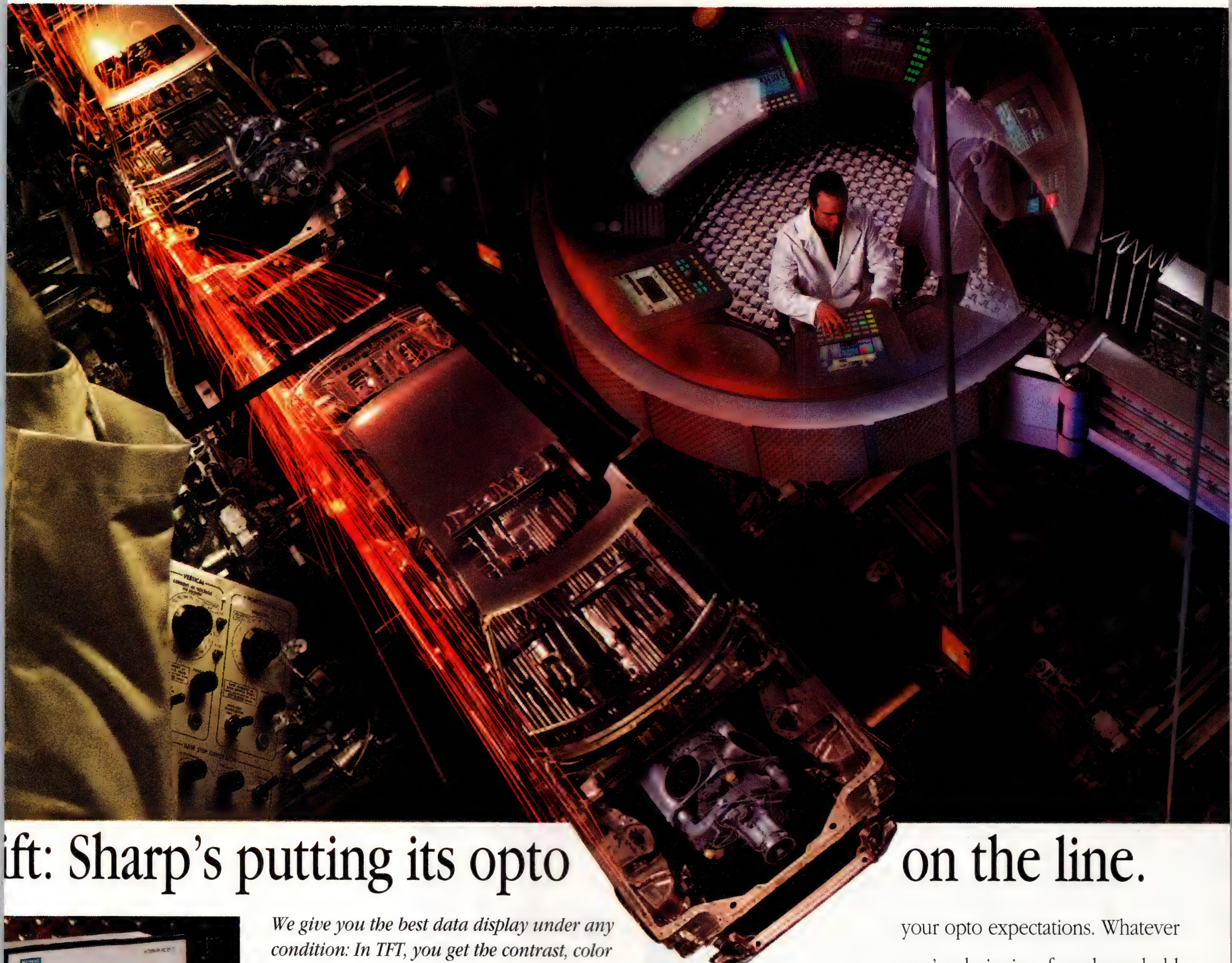

ift: Sharp's putting its opto on the line.

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single chip, to save space,
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Bipolar “T Switch” Minimizes The Problem Of All-Hostile Crosstalk In A Video Multiplexer

Professional video systems must be able to multiplex (select) between many input signal sources without suffering any interference from adjacent unselected sources. If the multiplexed signals are digitized, the task is simple because of the large noise margin provided in the digital domain. However, most video information is still multiplexed while it's in analog form to reduce the total amount of analog-to-digital conversion required.

If a video system is to be labeled “professional,” it must reject all non-selected signals by a margin of at least 72 dB. That is, all-hostile crosstalk interference must be at least 72 dB below the selected signal level. This level of isolation is difficult to achieve because the crosstalk effect degrades by 6 dB every time the number of inputs are doubled. In addition, video multiplexers have to provide wide bandwidth, low differential gain and phase, and must be able to switch quickly and cleanly so the signal sources can be changed “in picture” (between pixels) without visible lines or distortion coming into play. Until now, this task has demanded cascades of discrete switches and amplifiers.

To meet this requirement in a single IC, John Wright, a designer at Linear Technology, Milpitas, Calif., employed T switches built from high-speed vertical pnp transistors. In addition, he added gain-of-one input buffers before the switches and a current-feedback op amp after them, both of which (like the switches) take advantage of the company's high-speed and wideband complementary-bipolar process *(Fig. 1)*. The result is a family of video multiplexers that offer a typical all-hostile crosstalk specification of –92 dB at a frequency of 10 MHz.

Before the advent of high-definition TV, interactive CD ROM, and other forms of multimedia, as well as the proliferation of video-processing circuits, video sources were selected during a TV- signal's blanking period, and switching transients and crosstalk weren't visible. However, the latest video systems demand switching between pixels for “in picture” effects.

Earlier switching techniques simply don't work. For example, ICs using slow lateral pnp transistors (p-type devices are required to switch with TTL/CMOS logic) in the signal path take several microseconds to settle, thereby blurring the transition between pictures. In addition, CMOS analog multiplexers, which are bidirectional, suffer from poor output-to-input isolation and create transients that “feed” the inputs.

CMOS multiplexer circuits built with break-before-make switches eliminate crosstalk effects between channels. However, they suffer from output glitches large enough to interfere with sync circuits *(Fig. 2a)*.

The use of high-speed pnp-transistor switches can clearly eliminate these large glitches *(Fig. 2b)*. As can be seen in each figure, the logic input voltage consists of a 5-V square-wave signal (bottom waveform), the center waveform is the glitch on the multiplexer's input (due to the logic), and the top waveform is the glitch on the output. The vertical scale factor for the CMOS device's input and output signals is 1 V/div. On the other hand, the vertical scale factor for Linear Technology's multiplexer input is a mere 10 mV/div., and for the multiplexer's output it's 50 mV/div. That is, the bipolar device's glitches are an order of magnitude less than those of the CMOS multiplexer circuit.

The gain-of-one buffer circuits provided on each input and formed

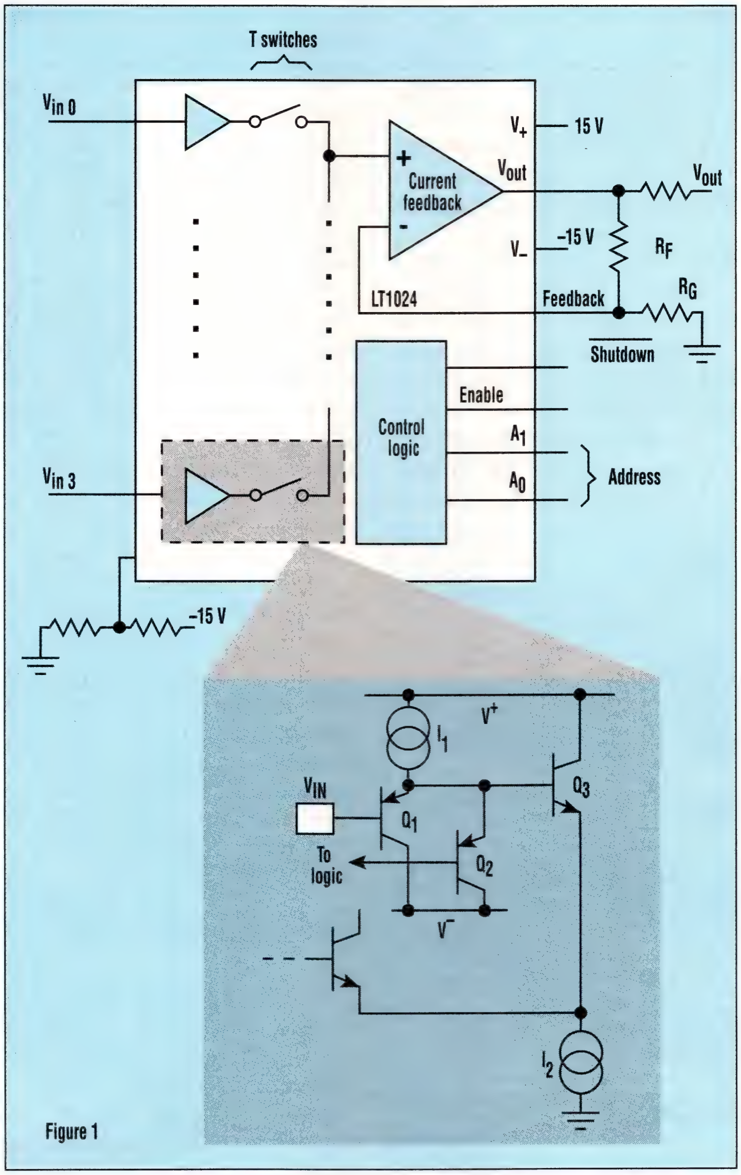
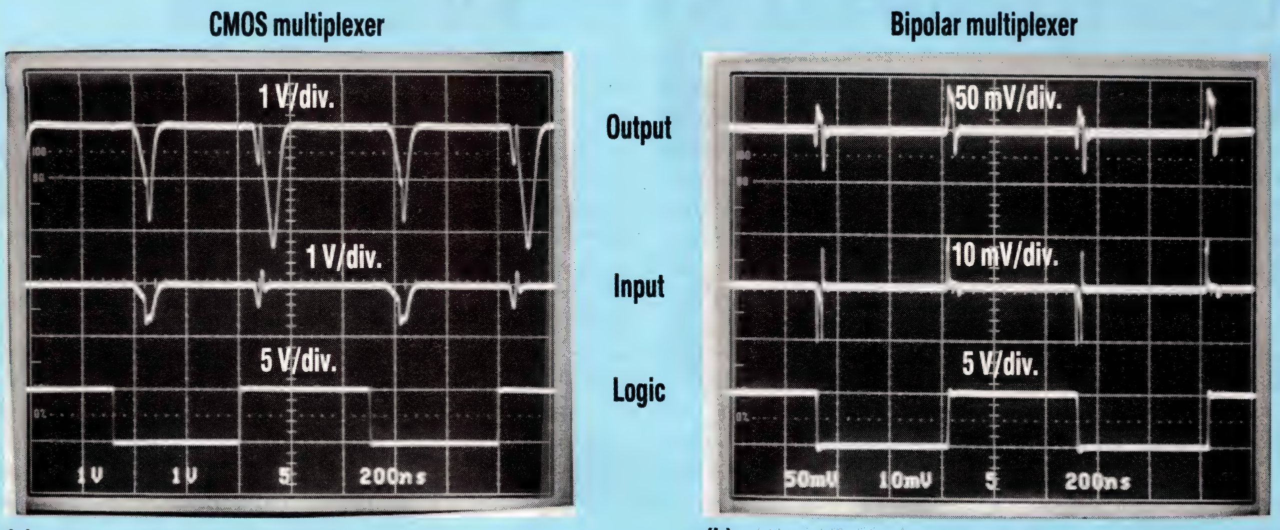


Figure 1



(a) 200 ns/div. (b) 200 ns/div.

Fig. 2

by pnp transistor Q_1 provide the isolation that keeps the glitch off the input *(Fig. 1, again)*. Without these buffer circuits, the glitch could interfere with other equipment connected to the signal source.

Careful design of these input buffer circuits included close matching of the dc characteristics as well as the ac performance. A dc-offset-voltage mismatch as small as 3 mV between channels can be visible on a high-quality video monitor. The multiplexers provide a channel-to-channel offset-voltage match of better than 300 mV.

Crosstalk is minimized within the T switch. When the switch channel is on (transistor Q_2 is off), transistors Q_1 and Q_3 form a pair of emitter-follower circuits with excellent ac performance to drive the op amp. When the logic circuits turn the switch off, the emitterjunctionsoftransistors Q_1 and Q_3 become back-biased and the emitter of transistor Q_2 absorbs current from current source I_1.

Current source I_2 routes signal current to any "on" switch. Users can set the multiplexer circuit's gain by selecting the value of the op amp's feedback and gain resistors R_F andR_G.

The type of die employed and the package layout used also minimize crosstalk, particularly if the multiplexer circuit is used with the recommended pc-board layout. For example, both the die and the package of the LT1024 video multiplexer IC contain a ground between each input, and the output and feedback pins are on one side of the 14-pin DIP or SOIC. Input pins of the four-channel LT1204 are located on the opposite side.

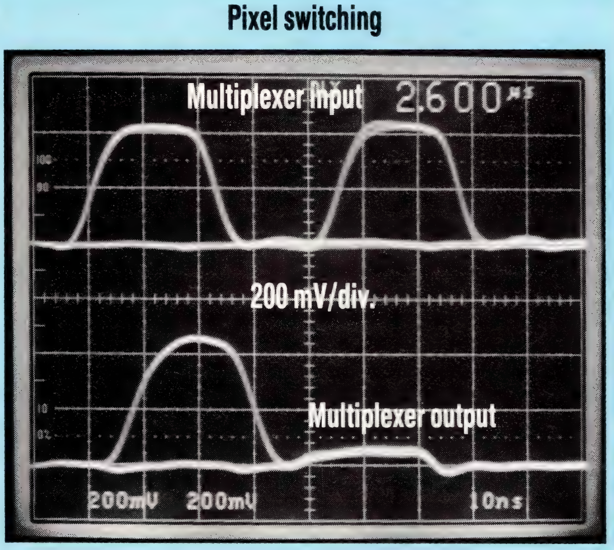
A reference-input circuit on the multiplexer device allows users to trade off the positive input-voltage range for a faster switching time. For instance, when running off ±15-V rails, setting the voltage level on the reference-input pin to –6.8 V cuts the switching transient time to just 50 ns. But it also cuts the input-voltage range from ±6 V to a lower value of +2.35 V to –6 V. When switching composite video "in picture" signals, this short transient becomes imperceptible on even the best monitors.

Performance of the LT1204 IC is well demonstrated by switching pixels *(Fig. 3)*. As can be seen, a channel carrying 22-ns pixels is shown selected, or turned on (left), and de-selected, or turned off (right).

The video mulitiplexer also has typical differential gain and phase of 0.04% and 0.06°, respectively, while driving a 150-Ω load (a doubly terminated 75-Ω line) and being powered from ±15-V rails. Even when running off ±5-V rails, differential gain remains at 0.04%, however differential phase increases to 0.12°.

For additional information, call Bob Scott at (408) 432-1900.

FRANK GOODENOUGH



10 ns/div.

Fig. 3

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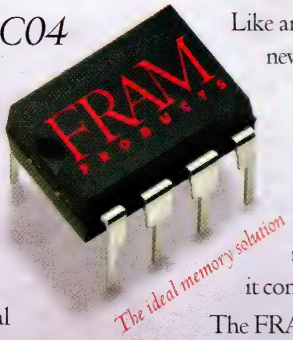

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24C04	Write Time	Active Power	Read/Write Endurance
FRAM	no delay	0.5 mW	100,000,000 cycles
EEPROM	10 ms	10.0 mW	100,000 cycles

RAMTRON

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READER SERVICE 118

Insulated Baseplate Enhances The Overall Efficiency Of Integrated Power Hybrids

For packaging engineers, different types of devices bring different kinds of challenges. With small-signal or logic ICs, the problems are related to issues such as signal delays, parasitics, and critical-path lengths. But when it comes to power hybrids, the emphasis is on efficiency.

In designing the package for its fledgling series of highly-integrated power-hybrid modules, Motorola's Semiconductor Products Sector, Phoenix, Ariz., had to shift its thinking. The company had to reorient itself from the low-voltage microcontrollers it typically encases in resin or ceramic materials to the insulated-gate bipolar transistors (IGBTs) that handle the heavier currents of 30 A and beyond and the higher voltages of 600 and 1200 V.

Motorola's Semiconductor Products Sector targeted a few well-defined priorities in the package's design *(see figure, inset)*. One priority was cost effectiveness, which dictated a hard look at materials and assembly steps. Another priority was the reliability of the IGBT and the rectifier silicon to be contained within the package—a function that's handled mainly by the thermal efficiency of the package's baseplate's .

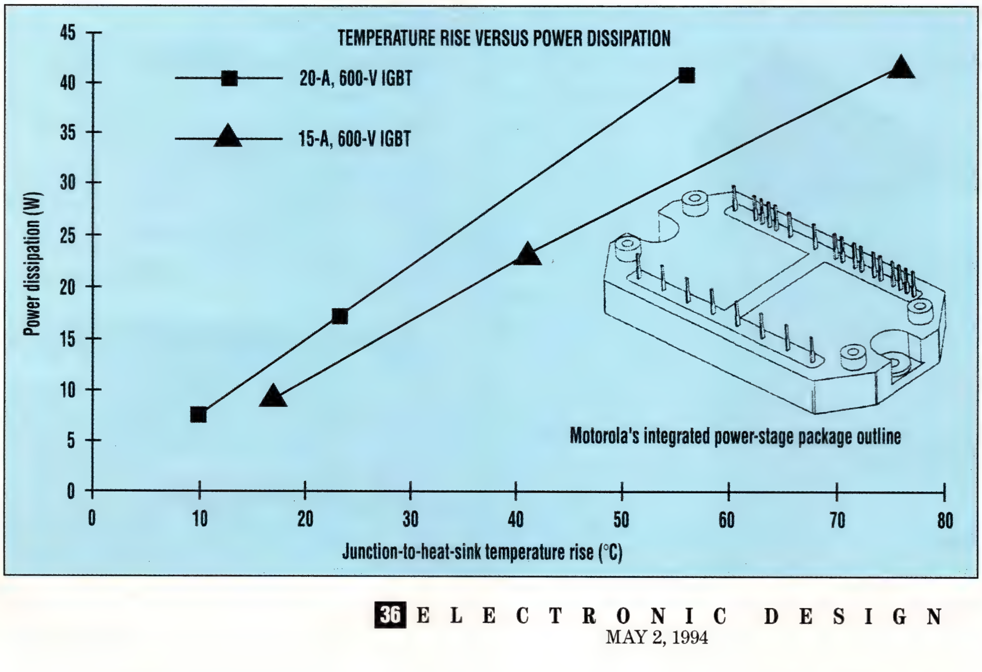
The basis for the package is an insulated metal baseplate system. The system consists of an aluminum baseplate and copper foil. A thermally-conductive layer of epoxy acts as an insulating layer between the two metals. An etching process forms the power-substrate circuit.

The silicon device is next bonded to a molybdenum or copper heat spreader. The following step is to connect the silicon-heat spreader subassemblies and the output leads to the power substrate. After the wire-bonding process, a plastic housing is attached to the substrate.

Once the circuit is assembled, the package is filled with a dielectric material called "Sil-gel" to above the height of the wire bonds. That step serves to protect the wire bonds and the die. Then the package is filled the rest of the way with a potting epoxy whose quality level is applicable to semiconductors.

According to Aristide Tintikakis, design manager for the hybrid power modules at Motorola Semiconductor, the difference between a hybrid module and a discrete motor-drive solution is one of higher power density. "The full power stage of a motor-drive system is much larger in a discrete solution," says Tintikakis. "Using TO-220 or TO-247 packages is not as efficient from a thermal standpoint."

In planning its packaging strategy, the design team at Motorola Semiconductor had to consider future extensions of the company's power-hybrid family. The earliest product introductions, slated for June and July of this year, are power-hybrid models that can handle 15 A at 600 V and 5 A at 1200 V, respectively. In the fall, versions rated for 20 and 30 A at 600 V are scheduled to be introduced. And, 10- and 15-A versions at 1200 V are expected before the end of the year.



Last fall, the Motorola design team evaluated the performance of a number of mechanical systems. Their conclusion was that the baseplate can handle motor-drive solutions that can range up to 5 hp. For a 460-V input, that means IGBTs that are rated at up to 25 A and at 1200 V. For 3-hp drives, it translates into IGBTs that can handle 30 A at 600 V.

The evaluation process involved extensive modeling of the thermal stack. The thermal stack is composed of the die, solder, heat spreader, baseplate, and the thermal resistance of the interface between the package and its heat sink.

The models revealed that the temperature increase on the IGBTs related to power dissipation was significantly lower than the maximum junction temperature sustainable by the IGBTs *(see the figure)*. As a result, Motorola expects to use the same packaging at higher power levels without impacting performance or reliability.

The company plans to expand its power-hybrid line into the high-power realm, which Tintikakis defines as greater than a 10-kW output, and eventually reaching as high as 500 kW. Utilizing advanced materials and techniques, Motorola is now working on a package design and manufacturing-process development for those power levels.

For further information, contact Bill Roman at (602) 244-3103.

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	4 Meg	x4	70, 80	Now
		x16	60, 70, 80	3Q94/4Q94
Synchronous DRAMs	16 Meg	x8	10, 12, 13	3Q94/4Q94
DRAM Modules	32MB	x32, x64, x72	60, 70	3Q94/4Q94
	16MB	x32, x64, x72	60, 70	3Q94/4Q94
	8MB	x32, x64, x72	60, 70, 80	Now
	4MB	x32	60, 70, 80	Now
88-Pin DRAM Cards and MiniCards	32MB	x32	60, 70	3Q94/4Q94
	16MB	x32	60, 70	3Q94/4Q94
	8MB	x32	70, 80	Now
	4MB	x32	70, 80	Now
SRAMs	4 Meg	x4, x8, x16	12, 15, 20, 25	3Q94/4Q94
	1Meg (revolutionary)	x4, x8, x16	15, 20, 25	Now/3Q94
	1Meg (evolutionary)	x1, x4, x8	15, 20, 25	Now
	256K	x1, x4, x8	12, 15, 20, 25	Now
Synchronous SRAMs	1 Meg	x18, x36	7, 10, 12, 15, 17	Now/3Q94
SRAM Modules	4MB	x32	15, 20, 25	4Q94/1Q95
	1MB	x32	20, 25	3Q94/4Q94
	512KB	x32	20, 25	3Q94/4Q94
	256KB	x32	15, 20, 25	Now
Synchronous SRAM Modules	512KB	x72	7, 10, 12, 17	Now/3Q94
	256KB	x72	7, 10, 12, 17	Now/3Q94

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READER SERVICE 102

1300-NM OPTICAL AMPLIFIER TO BOOST OPTICAL-NETWORK CAPACITY

An optical amplifier that could increase the capacity of existing fiber-optic telecommunications networks by as much as 50 times is being readied for production by Hewlett-Packard Co.'s Fiberoptic Components Operation (HP-FCO) at Ipswich, England. The amplifier was invented at the research laboratories of British Telecom plc. It uses a 20-m length of fluoride glass fiber. The fiber is doped with praseodymium ions, allowing it to produce a gain level of around 30 dB.

The amplification process is based on the transfer of energy from a local energy source to a 1300-nm light-bearing signal. The process is mediated by the praseodymium ions which are incorporated into a fluoride core within a length of fiber.

An external laser energy source is employed. The small solid-state laser emits light at 1047 nm, a wavelength that excites the praseodymium ions. As the two lightwaves travel together through the fiber, energy is transferred from the 1300-nm lightwave to the 1047-nm lightwave. Typically, the 20-m-long praseodymium-doped fluoride fiber is sufficient for amplification factors of around 1000.

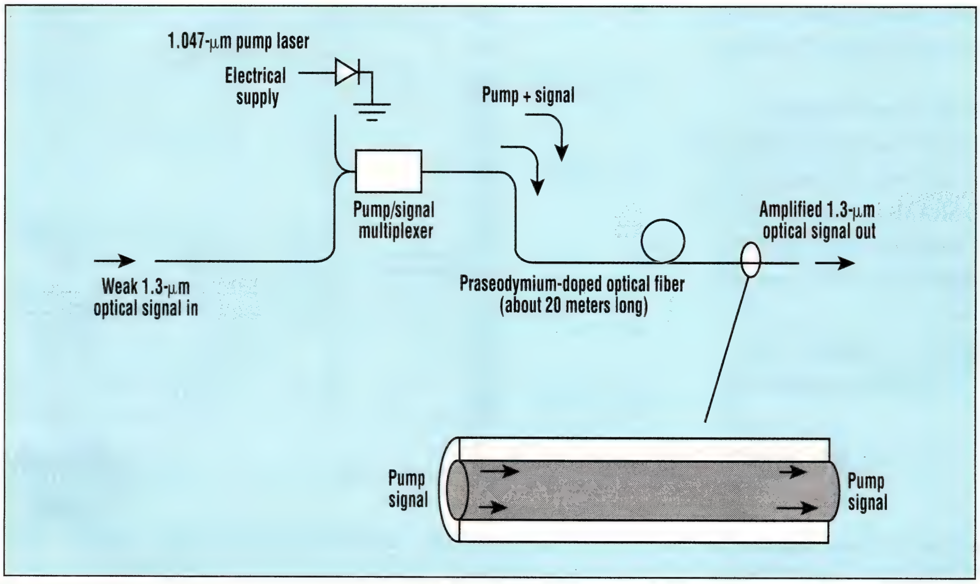
The fact that the amplifier can work on lightwaves with a wavelength of 1300 nm is important. Previous optical amplifiers using erbium-doped fiber only were able to work with 1500-nm lightwaves. Moreover, the amplifier operates on lightwaves directly without first converting them to an electronic signal.

Lesley Sweeney, business manager for advanced products at HP-FCO, explains that existing fiber-optic networks use optical fiber that's optimized for this wavelength. As a result, the new amplifier could be used to enhance these networks to meet the requirements for "information super highways" without the need to replace them.

The device's amplification is achieved by pumping the fluoride glass fiber with relatively high-power lightwaves. These lightwaves have a shorter wavelength of 1047 nm and emanate from a laser source composed of neodymium-yttrium-lithium-fluoride (Nd:YLF). The laser runs with an output power level of 1 W. The pump signal excites praseodymium ions within the fiber, and causes energy to be transferred to the signal-carrying lightwave as it travels through the optical fiber (see the figure).

Beside its gain, the optical amplifier has impressive performance specifications. These include a saturated output power level of +18 dB , a small-signal gain of 30 dB, and a noise figure that's typically 6 dB. Its small-signal bandwidth is 30 nm at a wavelength of 1300 nm.

The use of lightwave amplification overcomes dispersion problems in the older types of fiber. These dispersion problems limit both the range a signal may be trasmitted to around 70 km and the data rate at which the signal may be sent to 155 Mbits/s.


1.047-μm pump laser
Electrical supply
Pump + signal
Pump/signal multiplexer
Amplified 1.3-μm optical signal out
Weak 1.3-μm optical signal in
Praseodymium-doped optical fiber (about 20 meters long)
Pump signal
Pump signal

Using a prototype praseodymium amplifier, British Telecom plc demonstrated optical transmission rates of 5 Gbits/s over a distance of 100 km. This was achieved without any intermediate regeneration of the lightwave. However, according to the Hewlett-Packard Co., it will be some time before the new amplifier can be deployed in actual networks.

The first model of the new optical amplifier, designated the PFA-1000, is intended strictly for laboratory work, Sweeney explains. "I'd expect it to be another 18 to 24 months before it has been developed mechanically and it is ruggedized enough for deployment in a network environment, and for volume production," she says.

There are some engineering problems still to be overcome with this new optical amplifier. In particular, the praseodymium-doped fiber is extremely hydroscopic and vulnerable to moisture. As a result, a well-engineered hermetic package must be developed for the device before the optical amplifier could be deployed outside the labs.

Sweeney claims that British Telecomm plc and HP-FCO are the first to develop such an amplifier to the point where it can produced on a production basis. In fact, HP-FCO is taking orders at present. The company is currently quoting a price for the amplfiier of $75,000, and anticipates 16 weeks for its delivery.

For further information, contact HP-FCO in the United Kingdom at +44 (0)473 465315. In the U.S., call (302) 633-7458.

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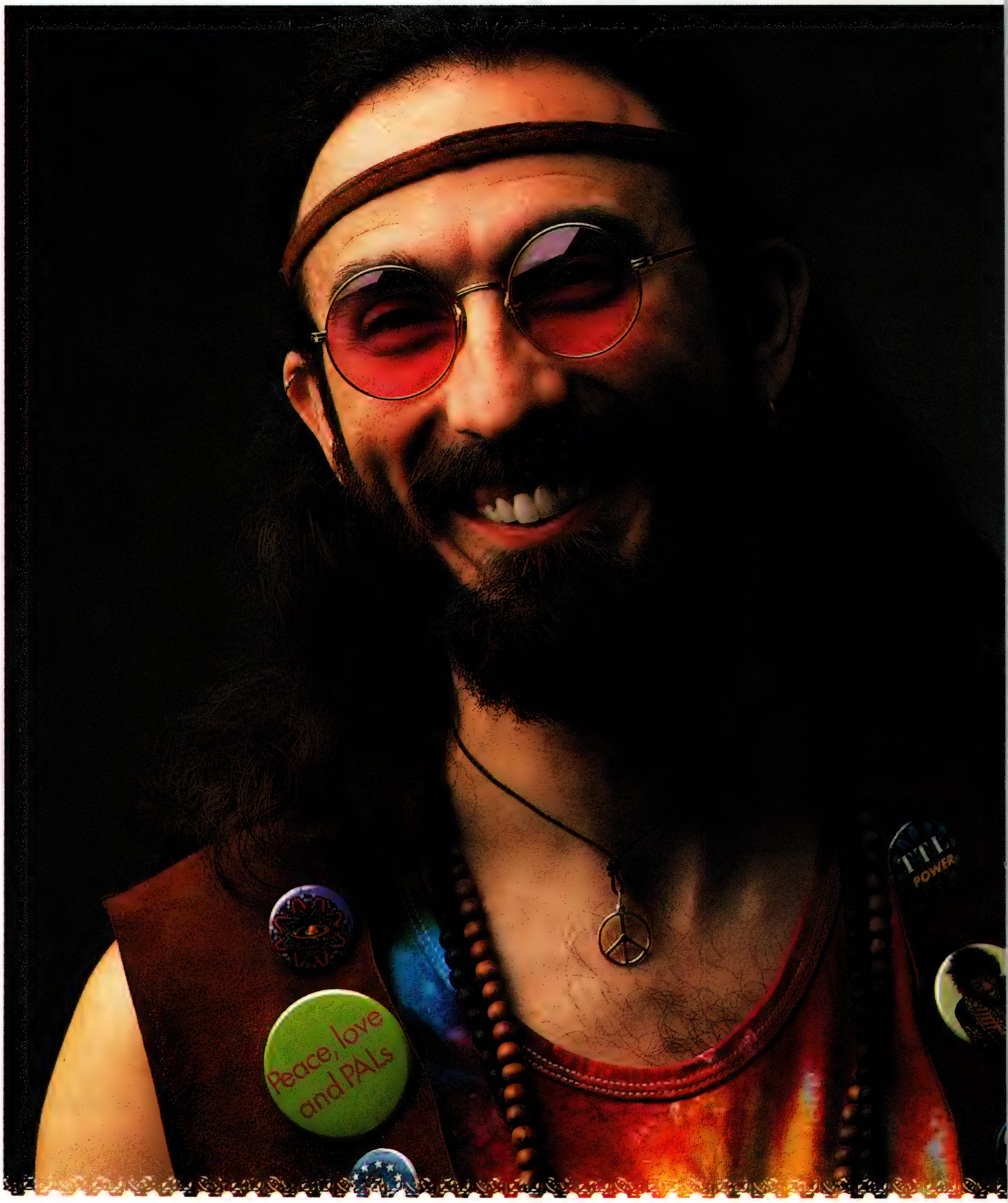

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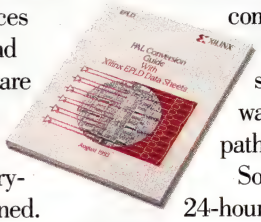

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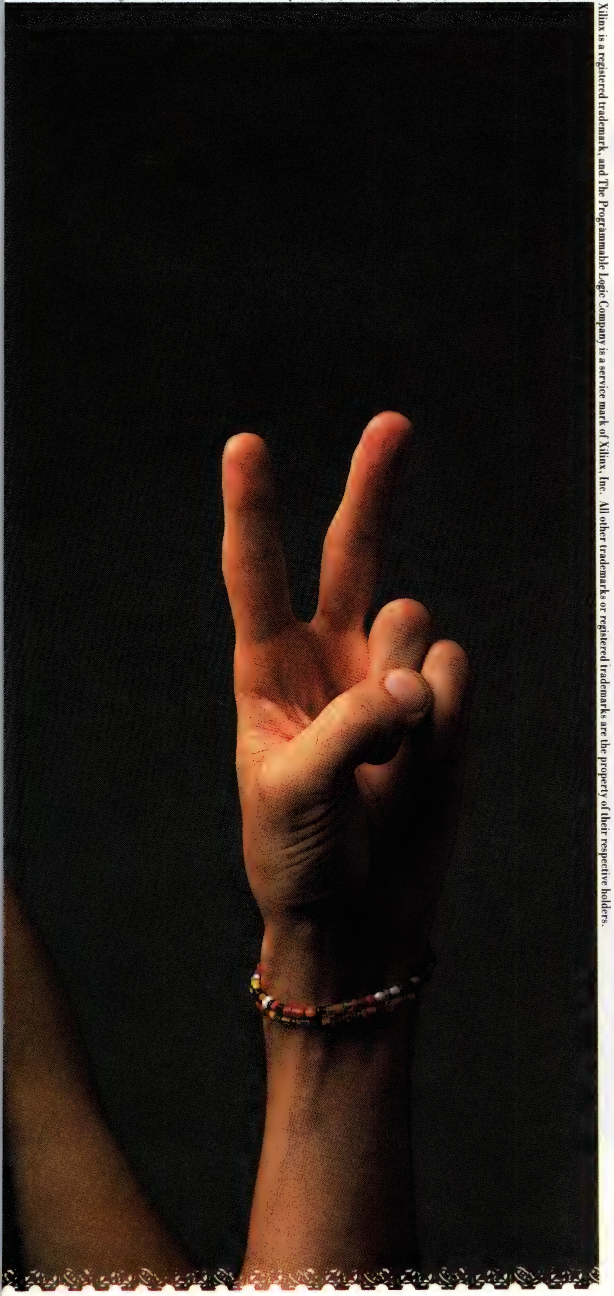

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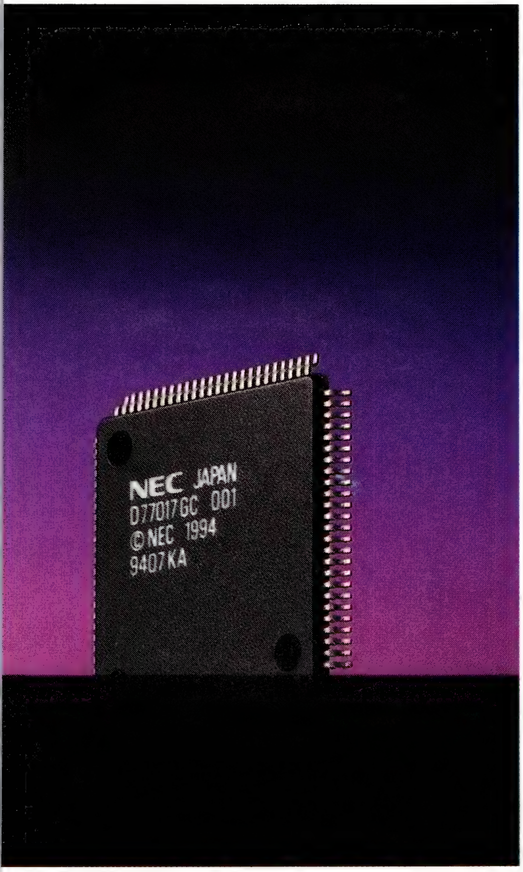
READER SERVICE 140

33MIPS
Optimized for
wireless
communications



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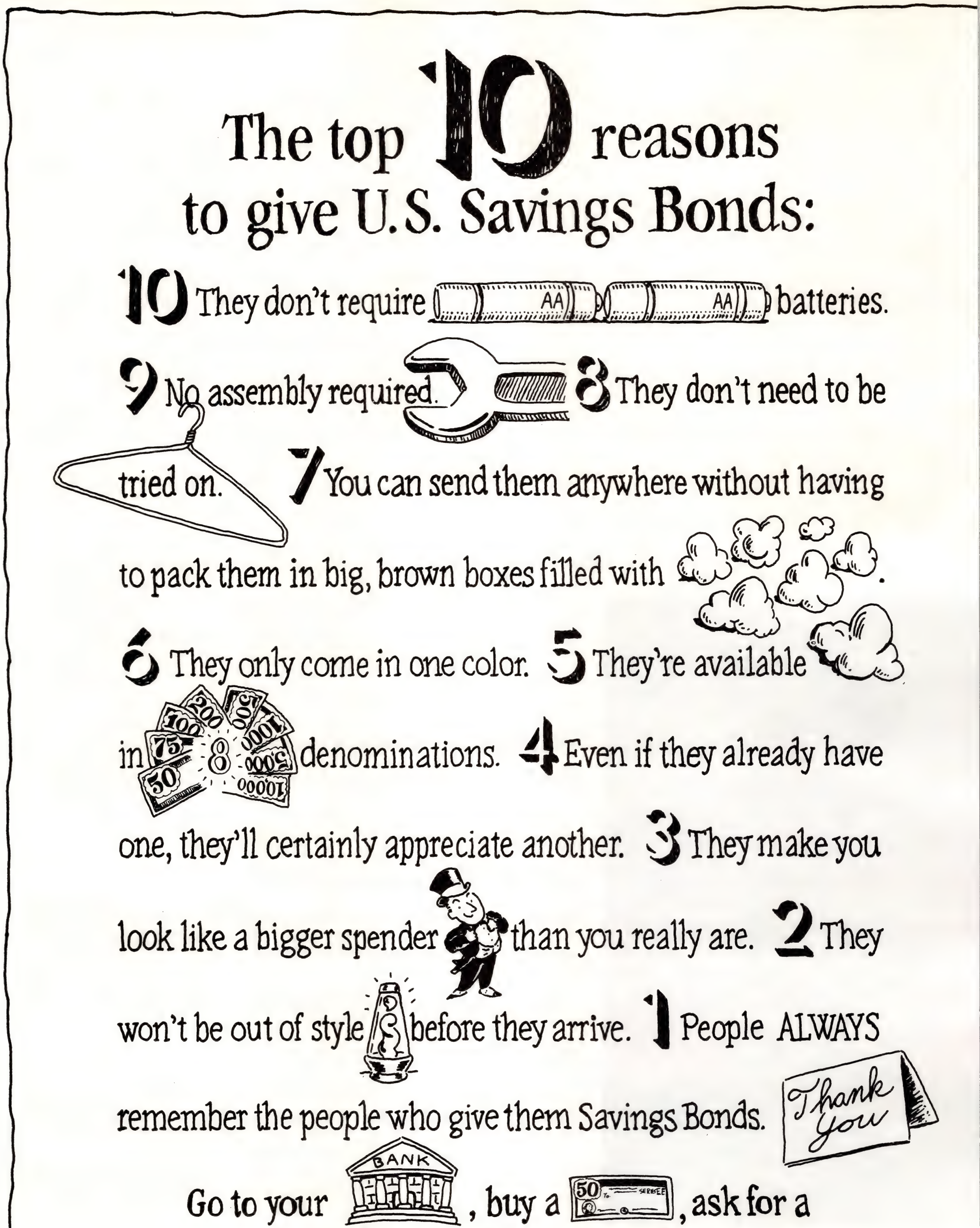

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CICC '94 examines the latest in ASIC designs

Continuing its tradition as *the* ASIC design conference of record, this year's 16th annual IEEE Custom Integrated Circuits Conference (CICC) unveils the newest in ASIC design developments. The conference's technical program includes 28 sessions (three of which are evening panel sessions) consisting of 144 technical presentations. As usual, a wide range of software and hardware subjects are explored. On the software side, numerous papers describe efforts to raise EDA high-level-design abstraction levels, and examine the latest in mixed-signal and physical design tools. On the hardware side, the latest in digital programmable-logic and high-speed signal-processing circuits is divulged. The emphasis here is on user-configurability and low-power consumption using CMOS processes. Similar low-power issues dominate the analog and mixed-signal hardware technical presentations, with many papers homing in on data converters, particularly the maturing delta-sigma designs. The other major arena, communications, is experiencing explosive progress, as is evident by the many advanced designs for DSP, data-communications, wireless, and RF circuits, wose performance levels are soaring to previously unthinkable heights. The conference is scheduled for May 1-4 at the Town and Country, San Diego, Calif.

1994 CICC TECHNICAL PROGRAM

Session 1 Keynote Address	**Session 2** Low-Power Custom Technologies	**Session 3** Topics in Simulation and Modeling	**Session 4** Signal Processing for Communications	**Session 5** Programmable Logic Architectures and Applications
Session 6 Video Compression and Consumer Applications	**Session 7** Synthesis for Digital Systems and Silicon	**Session 8** Analog Circuit Techniques for Communications	**Session 9** Advances in Programmable Logic Architectures	**Session 10** Application-Specific Digital Signal Processing
Session 11 Synthesis and Optimization	**Session 12** Low-Power, Low-Voltage Designs and Techniques	**Session 13** Statistical and Yield Modeling	**Session 14** Automotive and Sensor Circuit Techniques	**Session 15** Analog HDL and Synthesis
Session 16 Wireless Communications	**Session 17** Test and Reliability	**Session 18 (Panel)** The Semiconductor Industry and ASICs in the Age of Mega-Fabs	**Session 19 (Panel)** Has Analog Simulation Capability Fundamentally Improved in the Last Decade?	**Session 20 (Panel)** Cycle-Time Reduction: What is the Minimum?
Session 21 Mixed-mode Simulation and Behavioral Modeling	**Session 22** IC Fabrication Technology	**Session 23** Data Converters	**Session 24** Physical Design Analysis and Optimization	**Session 25** PLLs, Neural Nets, and High-Voltage Circuits
Session 26 High-Performance Memories and Gate Arrays	**Session 27** Broadband Communications	**Session 28** Physical Design for Advanced Technologies		

Low power tops the CICC agenda for analog and mixed-signal ICs

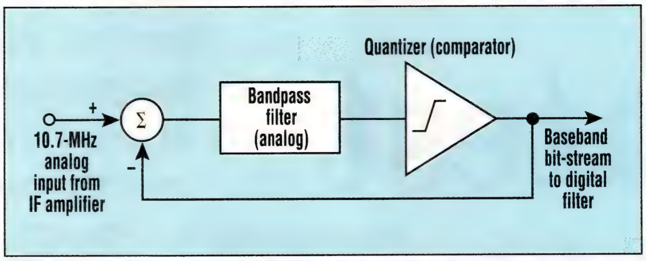
With interest widening in the use of delta-sigma ADCs, converters with ultra-low power-dissipation levels are coming of age.

BY FRANK GOODENOUGH

Low-power dissipation is the common theme among the analog and mixed-signal technologies and ICs described at this year's CICC conference. But, as evidenced by the conference papers, IC designers from systems houses, design groups, the academic world, etc., had to come up with this low-power dissipation without giving up speed or accuracy. They describe their efforts in tackling cell-based designs for custom and commercial ICs.

Like the annual International Solid State Circuits Conference (ISSCC) which preceded it, CICC's analog and mixed-signal technical papers are dominated by data converters—a total of nine. These converter designs also follow the trend set at the ISSCC of using delta-sigma circuits. The nine data converters break down into: four different delta-sigma (Δ-Σ) analog-to-digital converters (ADCs), a pair of low-power 10-bit video ADCs, a 12-bit/1-MHz, successive-approximation ADC needing just 1 mW of power, and a pair of low-power video digital-to-analog (DACs).

The remaining dozen or so analog/mixed-signal papers (plus several invited survey-type papers) describe a wide range of innovative circuit and process technologies. These ICs perform functions ranging from sensing magnetic fields to generating low-jitter 500-MHz clocks. They also include 5-V CMOS ICs that handle 50 V, a phase-startable 800-kHz-to-800-MHz relaxation oscillator built on a complementary-bipolar process, and an 800-MHz phase-locked loop (PLL) that mounts a GaAs chip on a silicon chip. Also included are several low-power digital prescalers that are able to handle logic inputs above 1.5 GHz, and a 560,000-pixel CCD image sensor for television.


Quantizer (comparator)
Bandpass filter (analog)
Σ
+
−
10.7-MHz analog input from IF amplifier
Baseband bit-stream to digital filter

1. ANALOG DOWNCONVERSION of IF signals followed by filtering at the baseband can be replaced by this bandpass delta-sigma modulator and a digital filter. The technique eliminates the need for passive LC tuning components.

A summary of the characteristics of the four Δ-Σ CICC papers, none of which aim at audio applications, shows that Δ-Σ designs have matured. Not only are very diverse devices appearing, they're also coming from a wide range of sources—not just one or two companies. The four devices include:

- A bandpass Δ-Σ modulator that operates at a center frequency of 10.7 MHz, provides a signal-to-noise ratio of 55 dB within a bandwidth of 200 kHz, and consumes just 60 mW.
- A complete 20-bit Δ-Σ ADC IC that achieves a dc-to-20-Hz bandwidth yet operates on a mere 2 mW.
- Four, 11-bit Δ-Σ ADCs on one chip that provide bandwidths of dc to 16, dc to 40, dc to 100, and dc to 200 Hz. Each draws just 300 μA at 3 V.
- A parallel Δ-Σ architecture in which multiple modulators connected in parallel operate on the same input signal to eliminate the need for oversampling.

There's wide interest in the use of ADCs, and Δ-Σ ADCs in particular, to digitize the output of a radio receiver's IF amplifier. The technique lets a DSP circuit perform both demodulation and filtering with sophisticated digital algorithms. A pair of designers, hailing from the University of Toronto in Canada, and Carleton University, Ottawa, Canada, built a Δ-Σ modulator IC for this task *(Fig. 1)*.

The IC was created to demonstrate the feasibility of replacing an analog heterodyne downconverter and an analog filter with a purely digital approach. In a bandpass Δ-Σ ADC, a bandpass noise-shaping filter replaces the usual low-pass circuit. This particular chip, with its 200-kHz filter at a center frequency of 10.2 MHz, aims at Groupe Speciale Mobile (GSM) cellular-telephone applications. The use of a digital filter at baseband eliminates external inductors or capacitors.

The second-order modulator employs switched-capacitor technology. Its quantization-noise-shaping filter is built with a pair of switched-capacitor bi-quads. Chips were built using two different filter characteristics: a "lossless discrete integrator" (LDI) and a "forward Euler" filter. The former design is less affected by capacitor mismatch, but it settles slower. The latter design settles faster, although it depends more on capacitor matching.

The bi-quad chips are built on a 0.8-μm biCMOS process. The filter's folded-cascode op amps employ both CMOS and bipolar devices. They provide 58 dB of gain, slew at 1200 V/μs, and are clocked at 42.8 MHz. With the exception of the nMOS input devices, which prevent loading of the previous stage, the op amps forming the latching comparator at the modulator's output are built entirely of npn transistors. The modulator provides 8-bit accuracy at 200 MHz.

One of the basic applications for Δ-Σ ADCs has been low-signal-frequency converters with a resolution of 16 or more bits. Two designers from Asahi Kasei Microsystems, one in Tokyo, Japan, and the other in San Diego, Calif., designed a complete

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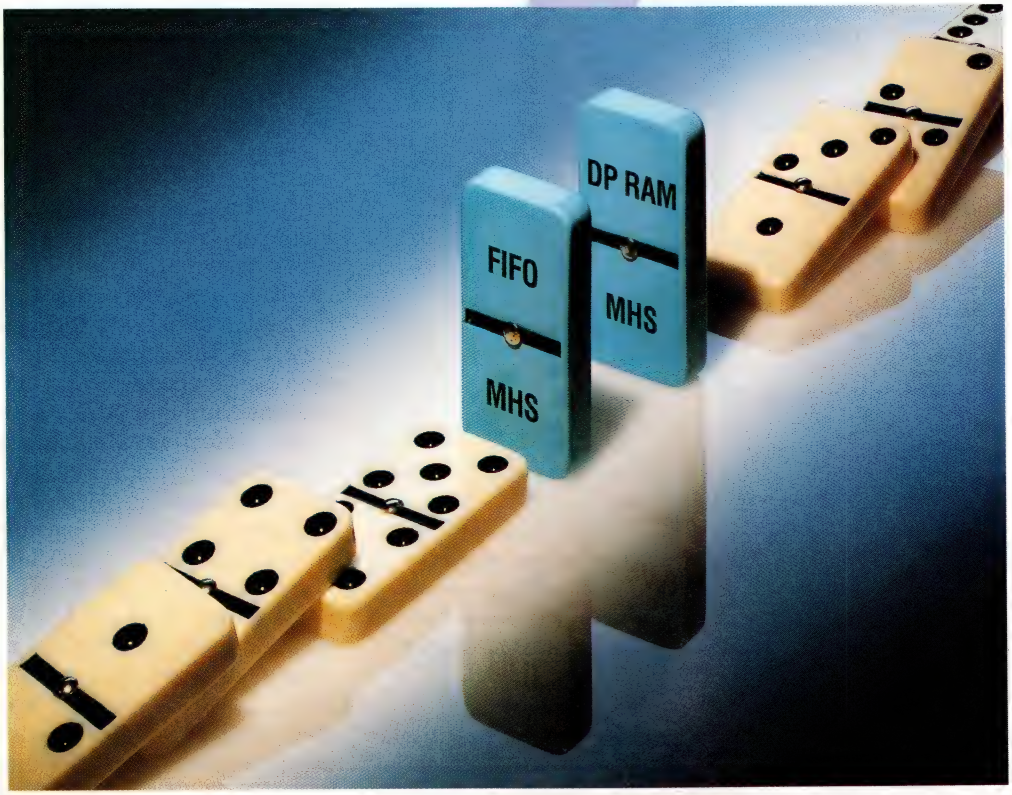

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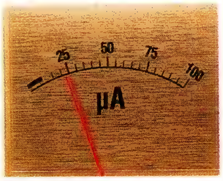

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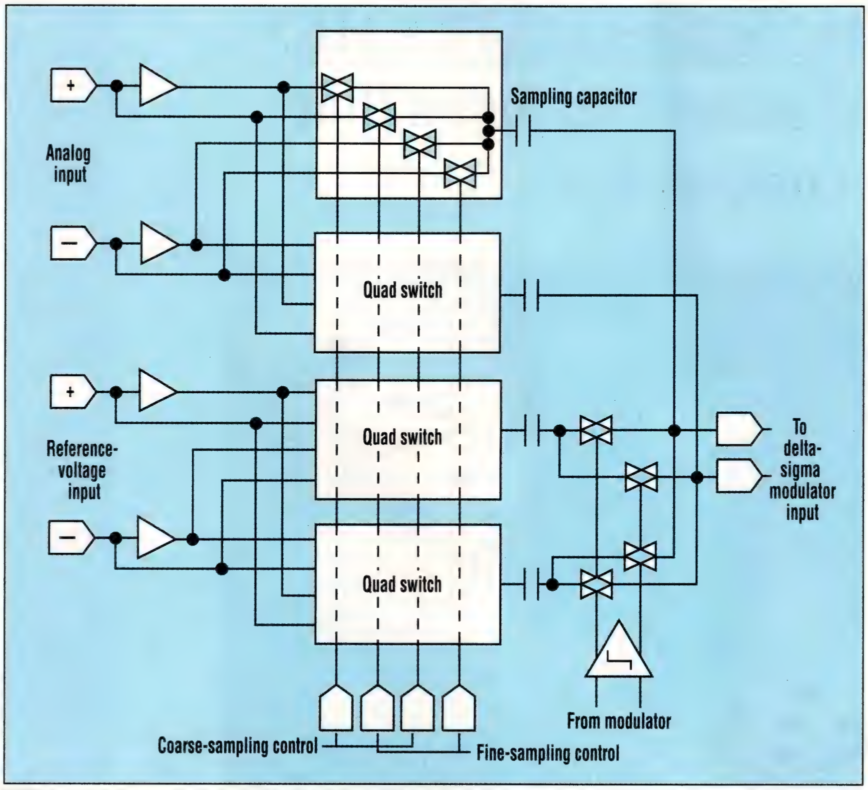


2. A HIGH INPUT IMPEDANCE CAN BE maintained without degrading accuracy by eliminating a buffer's offset error. This is accomplished in a 20-bit delta-sigma ADC that first coarse-samples, and then fine-samples, the input and reference. A buffer amplifier is employed in the signal path during coarse sampling. But during fine sampling, the inputs drive their sampling capacitors directly.

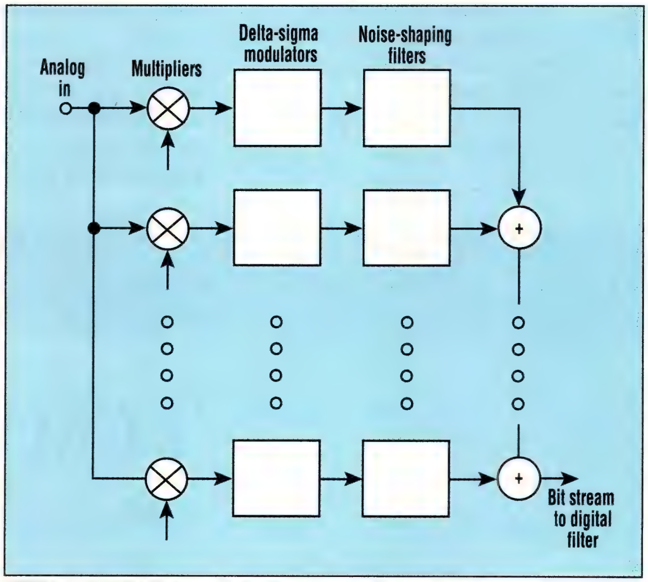
(modulator and digital filter) 20-bit Δ-Σ ADC on one chip. It operates at an effective sampling rate of 20 conversions/s and needs just 1.5 mW from a 5-V rail.

Because of the very low power consumption, it's well suited to digitize the output of remote sensors in process-control systems, where it could operate from a 4-to-20-mA current loop. The power dissipation is several orders of magnitude lower than what's available from any ADCs with similar performance.

The converter employs a fourth-order switched-capacitor Δ-Σ modulator. Signal flow is fully differential throughout to provide wide dynamic range while at the same time minimize common-mode switch-feedthrough and supply-rail noise. The first integrator stage is chopper-stabilized using a unique coarse/fine charge-transfer scheme *(Fig. 2)*. A 775-tap finite-impulse-response (FIR) filter removes the quantized high-frequency noise from the modulator's output. Th output is decimated to provide 16- o 20-bit user-selectable output codes It runs off oversampling clocks fro 32 to 256 kHz.

The ADC's coarse/fine samplin scheme retains a high input impedance while eliminating the noise an offset error that might be created b a series buffer amplifier. It als drops thermal noise (kT/C) 3 dB rela tive to the more common two-phas switched-capacitor sampling. During the first half of the sampling period, a buffered version of the signa and reference are stored on the sampling capacitors. Coarse sampling is followed by a "fine-sampling" perio in which the signal and reference ar connected directly to the capacitors Because the voltage adjustmen (and hence charge transfer) during the fine-sampling period is minimal a high "effective" input impedance is obtained. Logic inputs control coars and fine sampling. Offset and gai calibration also are provided. The chip is built from 1.2-μm CMOS.

A team from CSEM Neuchatel, Switzerland, built an ASIC that interfaces with four micromachined accelerometers. The sensors, the ASIC, a microcontroller, and a battery form a portable 3-axis shock-measurement system. Its function is to determine if "fragile" equipment or other goods being moved by common carriers were exposed to damage-causing shock.



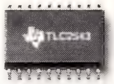
3. A NUMBER OF SECOND-ORDER delta-sigma modulators operating in parallel at low oversampling rates can replace a high-order device running at high oversampling rates.

The ASIC contains four analog front ends that interface with the four variable-capacitance accelerometers. Three of the front ends are followed by a programmable, switched-capacitor bandpass filter, a programmable window comparator, a Δ-Σ modulator, and a digital filter. The fourth front end is somewhat simpler. It consists of a filter, an rms-to-dc converter, and a window comparator. The chip also contains references, an oscillator, and logic circuits.

To save power, each axis can operate in a stop mode, a sleep mode, or a run mode. In stop mode, the amplifiers for each axis have no bias

What's the brightest news in A/D price and performance in 1994?

TI's new TLC2543 12-bit A/D converter at a 10-bit price.



he TLC2543 from Texas Instruments
ets a new price/performance point in
e marketplace. Its power dissipation is
nly 5 mW typical. That's 50 percent
wer than most 12-bit A/D converters, at
bout half the cost.

The right stuff. With the TLC2543
u get an on-board 14-channel multi-
lexer that offers 11 analog-input
hannels and three self-test chan-
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nd sample and hold. Plus a system
ock and 8-bit control register. And
 end of conversion flag makes it
asy to interface with microproces-
rs and DSPs.

TLC2543 Features

- 12-bit resolution A/D converter
- 10-µs maximum conversion time
- Low power consumption — 5 mW (typ), 13 mW (max)
- Power-down mode — 125 µW
- Standard serial interface
- On-chip system clock
- 11 analog-input channels
- Available in 20-pin SOIC, DIP or PLCC packages

New Members of TI's A/D Family

Device	Supply Voltage	Input/ Output	Conversion Speed (Max)	Resolution
TLC2543	5.0 V	11 ch/serial	10 µs	12 bits
TLV1549	3.3 V	1 ch/serial	21 µs	10 bits
TLC1549	5.0 V	1 ch/serial	21 µs	10 bits
TLV1543	3.3 V	11 ch/serial	21 µs	10 bits
TLC1541/43	5.0 V	11 ch/serial	21 µs	10 bits
TLC1550	5.0 V	1 ch/parallel	6 µs	10 bits
TLC1225	5.0 V	1 ch/parallel	12 µs	12 + sign

The TLC2543 in 3.3-V and shrink small-outline versions is on the horizon.

Where you need it. Use the TLC2543 in automotive, instrumentation and a broad range of industrial applications, including motor control, robotics, numerically controlled machine tools and data logging.

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1994 TI

00-8622ae

current, so they don't react to sensor outputs. In the sleep mode, only the analog circuits receive bias current—the window comparators are on, but the ADCs are off. When the comparators detect a shock, they wake up the rest of the chip. Channel gain is programmed in the filter over a range of 6 dB in 32 steps, while the bandwidth is programmed in 4 steps of 16, 40, 100, and 200 Hz.

The fourth Δ-Σ ADC, developed by a team from Washington State University, Pullman, and the University of California at Irvine, trades off the use of multiple parallel-connected Δ-Σ modulators against the need for oversampling *(Fig. 3)*. Called "parallel delta-sigma a-d conversion," the analog input is applied simultaneously to all of the modulators, each of which is followed by a conventional Δ-Σ modulator. The output of each is filtered and demodulated, and then all of the outputs are summed together to produce a single digital bit stream.

In a conventional Δ-Σ ADC, both the signal and the quantization noise pass through the same low-pass filter, and the low-pass decimation filter processes both. In contrast, the parallel Δ-Σ converters filter out much of the quantization error from the modulators without filtering the signal or oversampling.

The parallel approach achieves the resolution of higher-order Δ-Σ ADCs with relatively simple second-order modulators at low sampling frequencies. Running at low clock speeds also cuts power drain. Alternatively, the technique permits building simple high-speed, high-resolution Δ-Σ ADCs that run at high clock frequencies. The design team integrated 5 modulators on one chip and demonstrated a 16-channel device by connecting up multiple ICs.

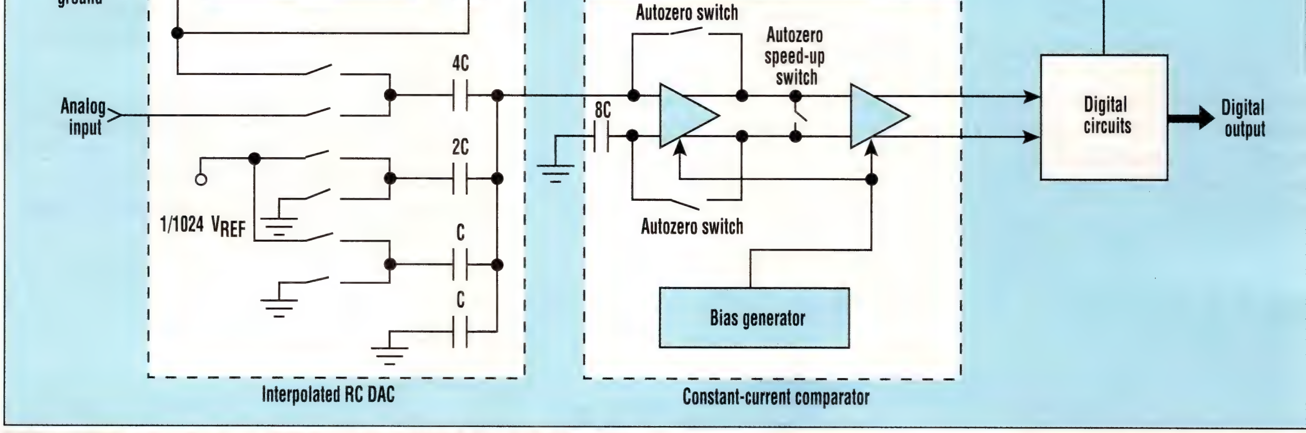
LOW-POWER 12-BIT ADC

A number of today's portable telecommunications and remote-sensor data-acquisition tasks demand low-power, 12-bit ADCs. With that in mind, a team of designers from Toshiba, Kawasaki, Japan, developed a 12-bit, 1-MHz ADC that consumes just 1 mW of power. The successive-approximation (SAR) design employs a unique DAC architecture and is built on a 0.8-μm, 2.4-mm-by-1.7-mm CMOS die.

The mix of high-speed, low-power, 12-bit resolution/accuracy on a small die required a trio of innovations: an interpolated resistor-capacitor DAC a high-speed decoder that controls the DAC, and a low-power, high-speed comparator *(Fig. 4)*. The interpolated RC DAC consists of a 10-bit segmented resistor ladder consisting of 1024 resistors and a 2-bit binary-weighted capacitor array.

The ladder's steering decoder is divided into upper and lower 5-bit decoders. Such partitioning was chosen to meet two preconditions. First DAC settling time depends on the ladder's parasitic capacitance. Second, guaranteed monotonicity must be independent of capacitance variation within a chip.

In a conventional decoder, the parasitic capacitance of 32 switches is connected to the output of the upper 5-bit decoder, thus increasing its settling time. In the new decoder, a single switch replaces a conventional decoder's 32-switch load, minimizing settling time. The first stage of the 2-stage comparator is autozeroed. The second stage takes the fast low-level output from the first stage to logic levels without degrading speed. The autozero period is shortened to gain additional speed by connecting the differential outputs of stages 1 and 2 together during the autozero period.



4. THIS 12-BIT, 1-MHZ ADC, WHICH EMPLOYS a successive-approximation architecture, needs just 1 mW of power from a 3-V supply rail. At the core of the ADC is an interpolating DAC with a 10-bit resistor ladder for the most-significant bits. This is followed by a 2-bit binary-weighted capacitor network for the least-significant bits.

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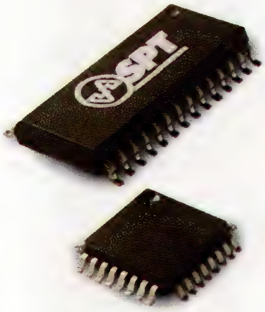

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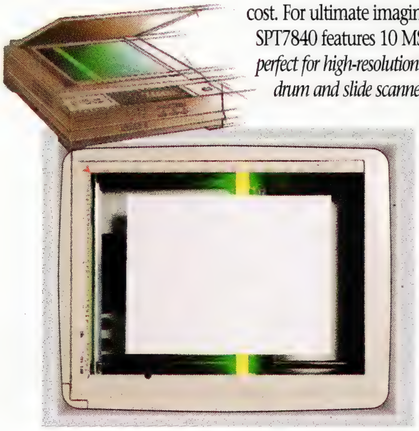
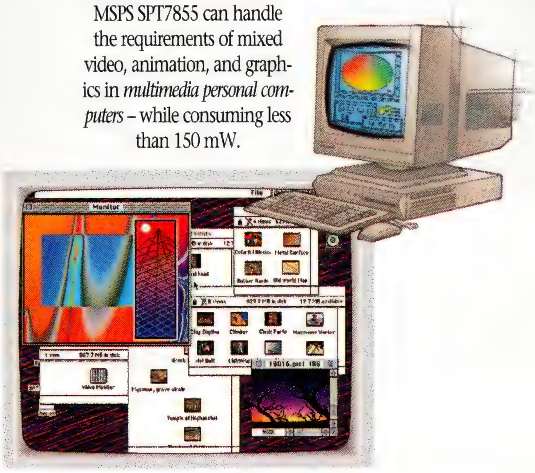


The 20 MSPS SPT7850 and 25 MSPS SPT7855 can handle the requirements of mixed video, animation, and graphics in *multimedia personal computers* – while consuming less than 150 mW.



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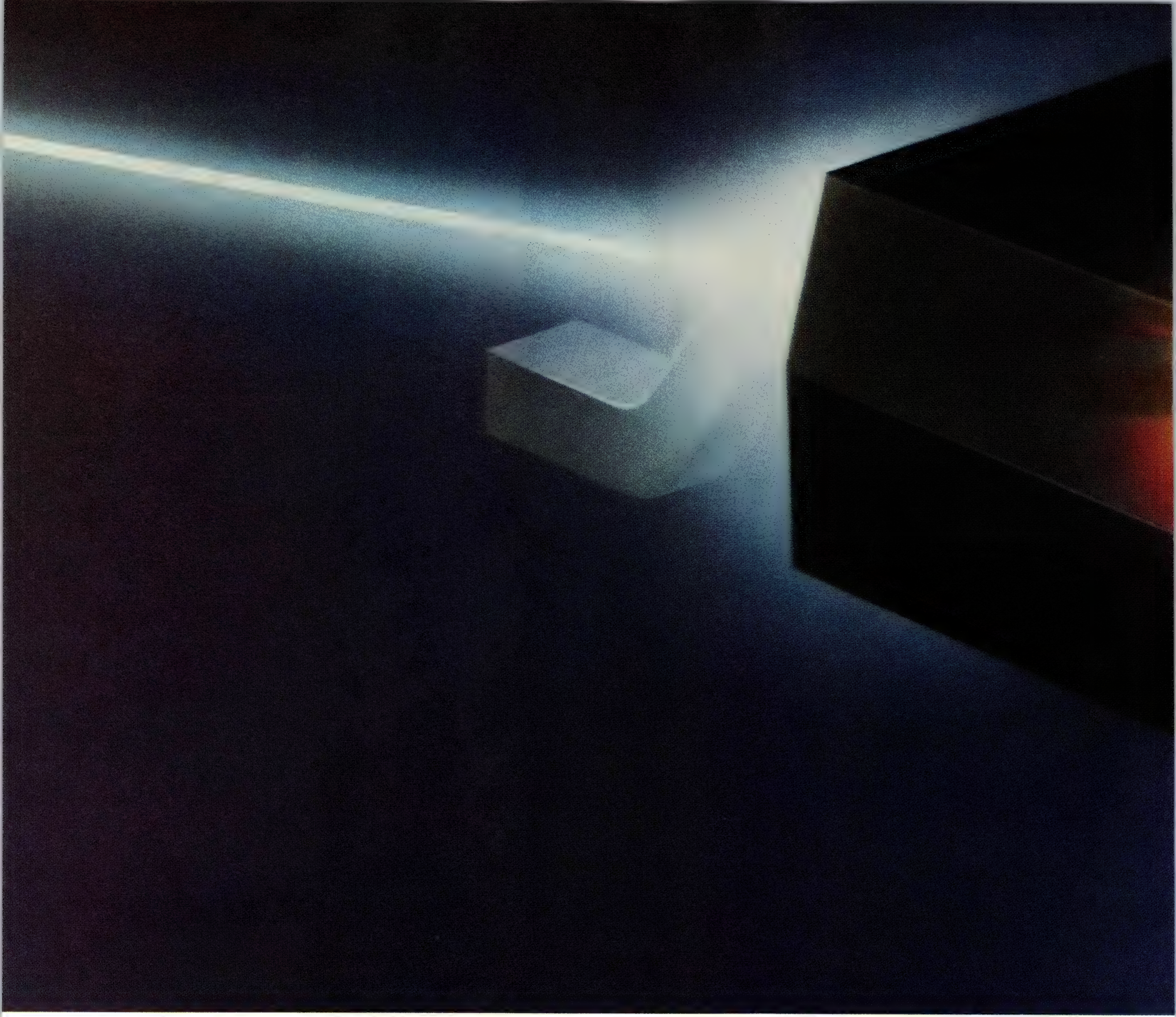

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SPI		1K	2K	4K		16K			
PARALLEL								64K	256K

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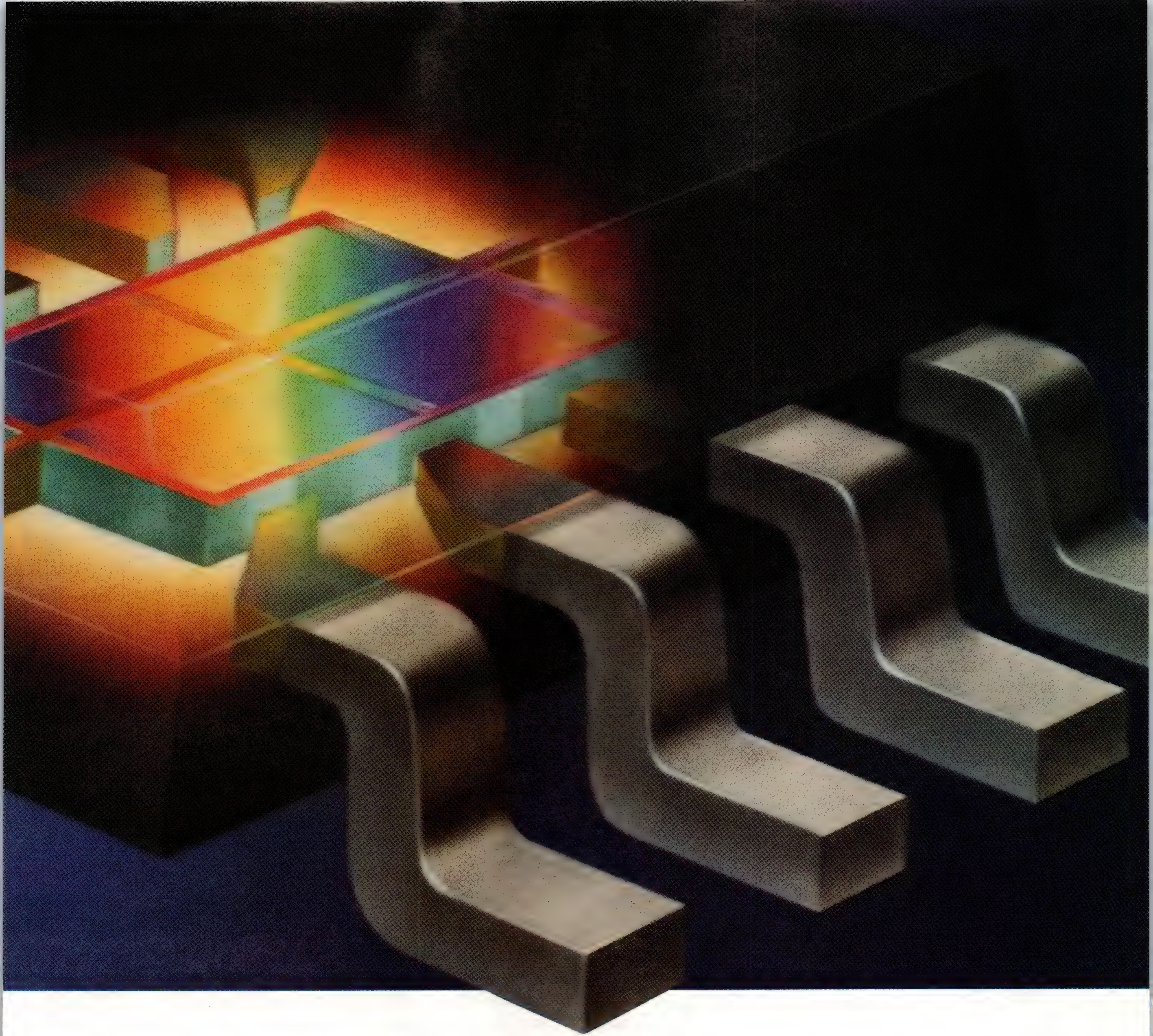

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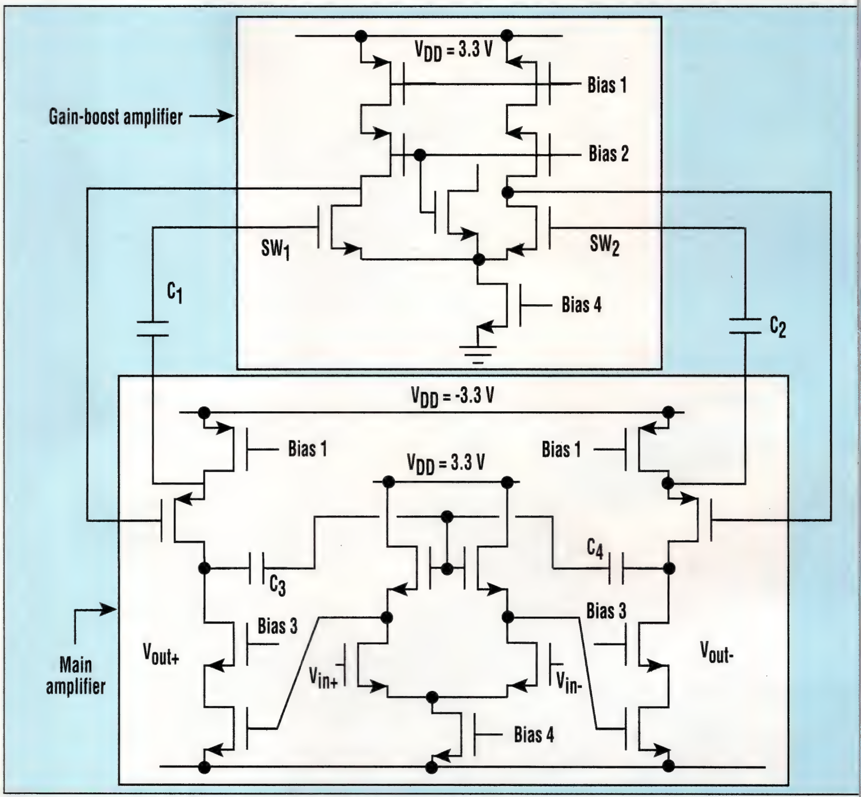
Comparator power consumption is minimized by running it in a constant-current mode. The IC draws 333 μA from a 3-V rail.

The final ADC reported at CICC, developed by a team of researchers at the University of California at Berkeley, provides 10-bit samples at 20 MHz yet needs only 35 mW of power from a 3.3-V rail. Using a pipelined design, the converter is built on a 1.2-μm CMOS process and provides 59.1 dB of SNDR (signal-to-noise plus distortion ratio) with a 100-kHz input signal. At the Nyquist rate, SNDR drops only 4 dB.

The pipeline contains nine, 2-bit flash quantizers, eight interstage amplifiers, and digital error-correction circuits. Power was saved by running off 3.3-V rails and minimizing the capacitive load on each op amp. The converter employs a number of neat circuits, many required to lower power and operate from the low-voltage supply.

For example, the MOS transmission gates used in each stage's sampling amplifiers and other switched-capacitor circuits don't work well at low voltage because insufficient gate drive is available. As a result, a unique charge pump is employed to raise the 3.3 V to 5 V for the transmission gates.



5. MORE AC GAIN CAN BE OBTAINED from this op amp's main amplifier by closing switches SW_1 and SW_2. This in turn adds the gain of the gain-boost amplifier via capacitors C_1 and C_2.

The 3.3-V supply rail puts very heavy demands on the chip's op amps, which must combine speed and high gain with an output swing as close as possible to the supply rails. The designers chose a two-stage circuit. The first stage, a low-gain preamplifier, raises the effective g_m of the second stage to provide fast settling. Series-feedback gain-boost amplifiers are included in the pMOS current sources to increase voltage gain *(Fig. 5)*. These amplifiers are capacitively coupled into the signal path with level-shift capacitors C_1 and C_2. They're initialized by closing switches SW_1 and SW_2. Capacitors C_3 and C_4 provide the common-mode feedback.

Additional power was saved by using small sampling capacitors in the latter stages of the pipeline. The larger the capacitor, the lower the kT/C, or thermal noise, created by the stage. But the larger the capacitor, the more power required by the op amps that drive them. However, the speed and accuracy requirements become less stringent towards the end of the pipeline, permitting smaller capacitors in that portion of the circuit.☐

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SLIGHTLY	538

CICC spotlights the struggle to raise EDA abstraction levels

Advances in high-level design stand out in a technical program that also reveals the latest in mixed-signal and physical tools. **BY LISA MALINIAK**

The ongoing struggle to raise the level at which engineers design draws much of the attention at this year's Custom Integrated Circuits Conference (CICC). To cope with the increasing size and complexity of ICs, as well as the shrinking design-cycle times, engineers are looking to design ICs at higher levels of abstraction. That's reflected in the technical program focusing on electronic-design-automation (EDA) tool advances, which includes many papers on synthesis technology and high-level analysis. The program

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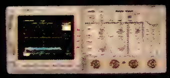
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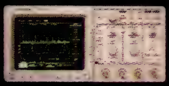
[TDS 420]
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[TDS 520A]
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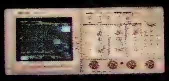
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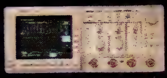
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also involves papers in other important areas, such as mixed-signal simulation and physical design.

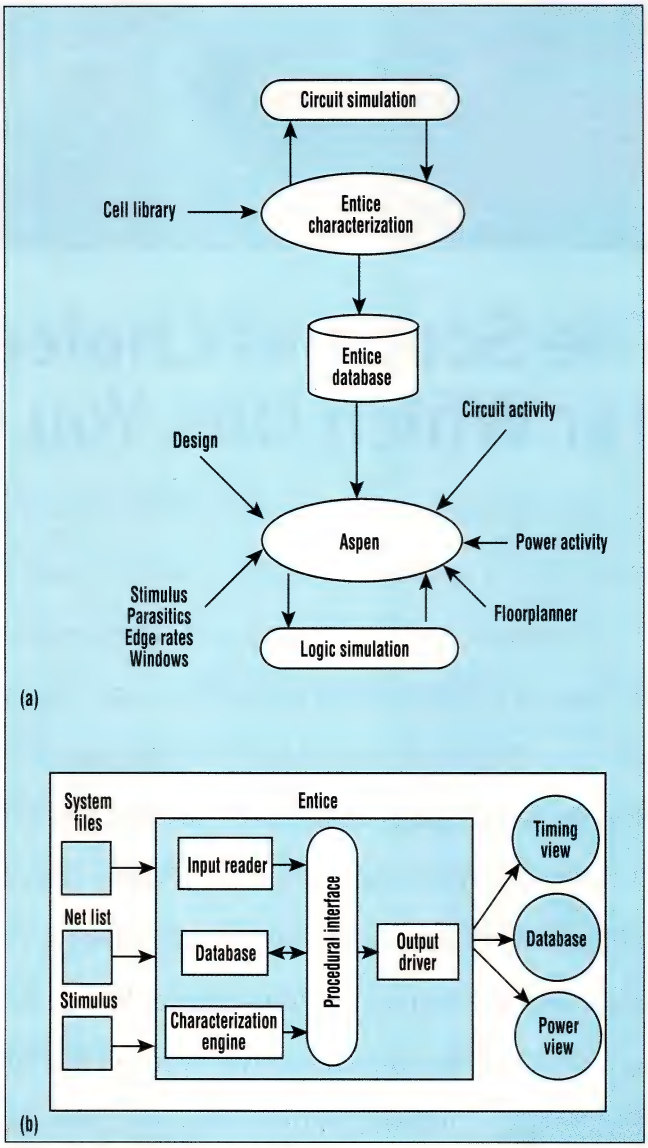
Session 7, which is dedicated to synthesis for digital systems and silicon, starts off with an invited paper from Redwood Design Automation Inc., San Jose, Calif. The paper dips into the past to predict the future of electronic-system-design-automation (ESDA) tools.

Generally speaking, there's much disagreement about what constitutes a system, let alone a system design tool. In the Redwood paper, entitled "EDA and Electronic System Design," the author defines a system as a collection of functionality implemented using electronics, including software and hardware. System design tools are most commonly thought of as concentrating on the higher-level functionality problem.

Three elements drive the need for this new area of EDA. The first is function mapping, which is the ability to map functions onto large preexisting library elements. One example involves mapping a function onto a CPU by generating software for it. The second element is protocols, or the movement and computation of data over time. In this case, time is measured symbolically rather than in absolute terms. The last area is structured data. ESDA will be built around the ability to describe the structure of large data objects, such as a video screen or an Ethernet packet.

The author's ESDA tool predictions include discussions of design entry, libraries, analysis, visualization and debug, controls, and output. For example, ESDA tools most likely will offer a mix of text and graphics for design entry. In addition, the ESDA level will exploit many small languages focused on a particular problem domain, such as dataflow descriptions for DSP design. What's not yet available is notations for describing protocols—data and computation spread over time.

The paper points out that libraries have developed into a thorny issue at the ESDA level. The best approach is to take an object-oriented look at large functions, which reveals that they have some internal state as well as several publicly available methods for getting the function to operate. The key is to come up with a common set of function definitions to create an abstract library element that implements an idealized version of the function. For instance, a library might contain five different UARTs. The abstract UART would define a set of methods to reset, initialize, set baud rate, send character, and so on.



1. A POWER-ANALYSIS environment devised by Motorola is based on the Aspen power-estimation system for cell-based CMOS designs, and the Entice semicustom cell characterization system for timing and power (a). With these two tools, it's possible to determine the static and dynamic power consumption of a circuit using power vectors. Entice offers accurate power-dissipation models for the user-specified parameters of interest (b).

SYNTHESIS LIBRARIES

The quality of a synthesized design depends on three interdependent components: the synthesis tool, the place-and-route tool, and the target cell library. Another paper in Session 7, titled "Improving Cell Libraries for Synthesis," from Synopsys Inc., Mountain View, Calif., discusses how to improve circuit speed by building a cell library. The authors suggest several library modifications, and explain how they constructed a "golden" library to verify their principles.

Two general cell-library modifications can help create a cell library that's well suited as a target for automated synthesis. The authors focused on principles with the greatest impact on improving circuit speed, yet they note that other principles should also be considered to improve parameters such as area and power.

The first modification involves multiple drive strengths. It's important that each cell in a library have a variety of drive strengths. Providing cells with only one drive strength can degrade circuit speed by 15 to 25%. It's particularly important to provide a wide range of drives for buffers and inverters.

Cell libraries also need dual polarities. Dual polarity means that both the logical function and its inversion are available as outputs of the same cell. For example, a single cell that has

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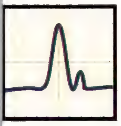

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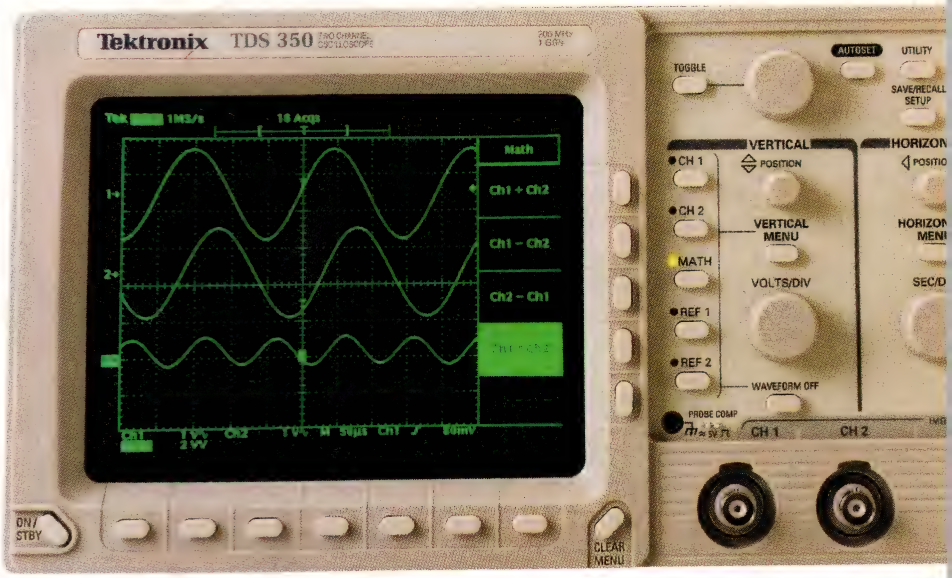

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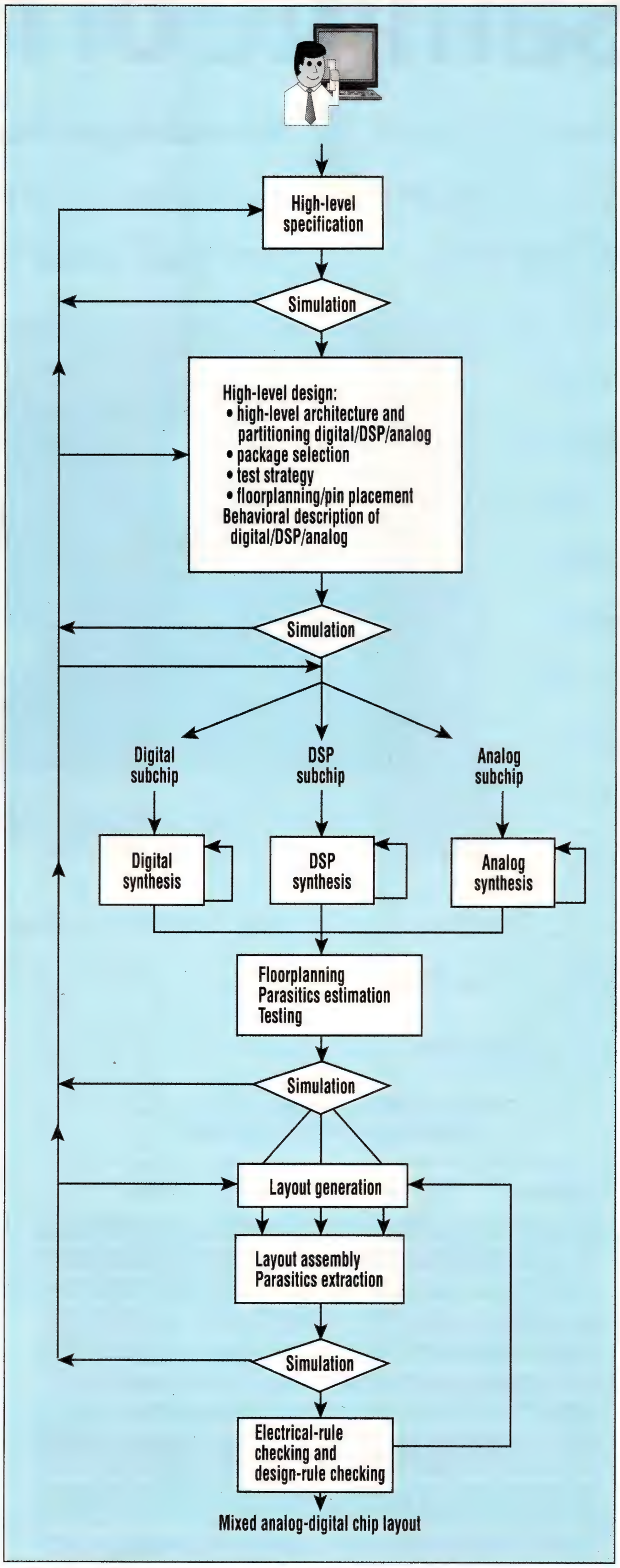
both NAND and AND functionality is a dual-polarity cell. Providing cells with dual polarity also implies that if the library offers NAND cells, it also should offer corresponding AND cells in the same sizes and drive strengths. In synthesized designs, high percentages of signals are required in both their inverted and noninverted polarities. Providing dual polarity actually improves area as well as improves speed.

One reason that dual-polarity cells and multiple drive strengths are important to synthesis is the growing significance of wiring delay in the overall circuit delay. Incorporating inverters and buffers into a circuit add not only the extra cells and their intrinsic delays, but also add extra wiring. Subsuming this wiring in a complementary (in the case of dual polarities) or higher-drive (in the case of multiple drive strengths) cell can reduce the interconnect delays, improving overall circuit speed. The impact of these principles will become more pronounced as mainstream design progresses deeper into submicron process technologies, and the resultant delay due to wiring becomes even more significant.

Session 11 also covers synthesis tools, and actually contains papers detailing both synthesis and optimization, such as is the case with power optimization. Measuring power consumption is critical for low-power design, because it enables designers to meet power specifications, drive power-optimization tools, distribute power effectively through a design, and choose appropriate packages. A paper from the Advanced Design Technology division of Motorola Inc., Tempe, Ariz., describes its power-analysis software for semicustom design.

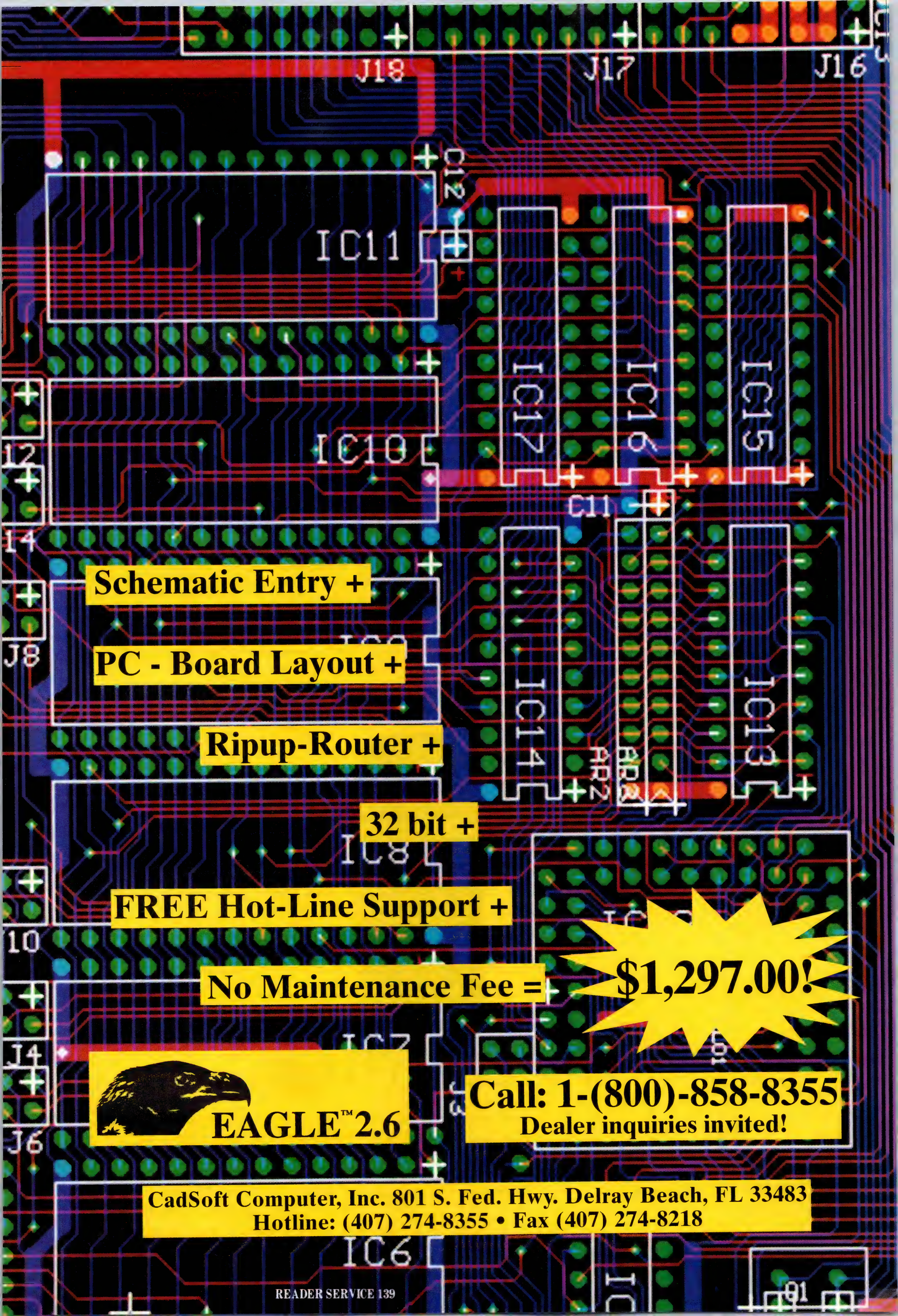


2. THIS DESIGN FLOW developed at Katholieke Universiteit, Leuven, Belgium, helps automate high-level synthesis of a mixed-signal ASIC's analog section. An architecture is generated from an analog behavioral description, and specifications are set for the modules within that architecture.

The Motorola system operates on a cell level, making it a faster alternative to the currently available transistor-level systems. It will calculate both static and dynamic power consumption of a circuit. Implementation results show that the Motorola system is four orders of magnitude faster than possible with circuit-level simulation, and achieves accuracy within 10% of the circuit-level results.

Power analysis is based on the Aspen power-estimation system for cell-based CMOS designs and Entice, a semicustom cell characterization system for timing and power *(Fig. 1a)*. With these two tools, it's possible to determine the static and dynamic power consumption of a circuit using power vectors, thereby providing accurate estimates over a wide range of realistic operating conditions. Before layout, this information can be used to produce macrocell power information, and then be used in floorplanning to balance power consumption on a chip. After layout, the analysis can calculate power consumption with back-annotated delays and actual wire loads.

The Entice-Aspen power-analysis system operates at the logic level. Entice provides accurate power-dissipation models for the user-specified parameters of interest *(Fig. 1b)*. Aspen makes it possible for designers to obtain power estimates for cell-based designs represented at the gate level. Existing sets of power vectors then can be employed to estimate the design's power consumption at different levels of the circuit hierarchy. This information eventually will as-



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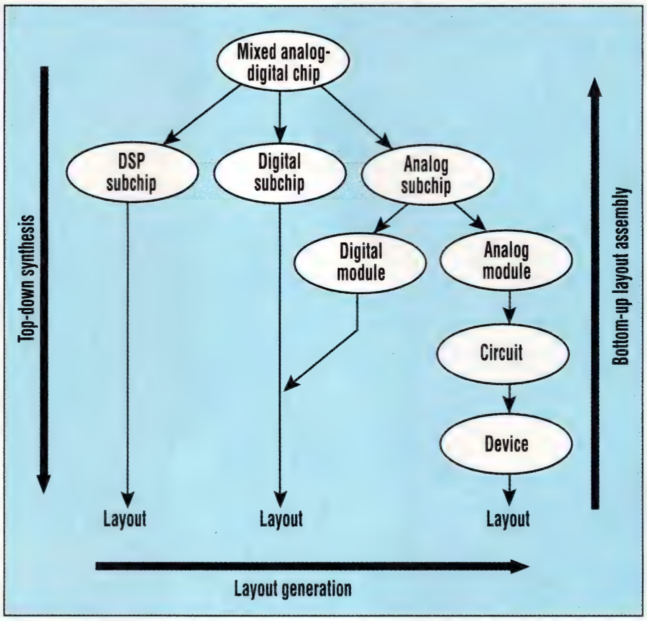
sist in the floorplanning and packaging decision-making process.

Aspen couples the circuit-activity information obtained from running a logic simulation with the Entice power - characterization data to calculate the three crucial components of power dissipation. They are the static power consumption due to leakage currents, dynamic power consumption due to short-circuit dissipation (caused by cell inputs switching), and dynamic power consumption due to capacitive dissipation (primarily interconnect charging and discharging).

The Aspen software acts as a turnkey system that fits easily into an existing CAD flow and provides functionality previously unavailable to the designer. As logic-synthesis technology advances to provide optimization for power, Aspen will be able to provide quick estimates of power consumption, giving designers concrete feedback about the success or failure of a synthesis compilation.



3. HIERARCHY MUST BE USED to master the complexity of designing a mixed-signal chip, but major differences exist between the hierarchies employed in the digital and analog domains. Analog hierarchy isn't based on signal abstraction, but rather on a structural decomposition over different levels.

ANALOG SYNTHESIS

Session 15 covers yet another aspect of synthesis technology—the dynamic area of analog hardware description languages and synthesis. A paper titled "A Methodology for Analog High-Level Synthesis," from Katholieke Universiteit Leuven, Belgium, presents a methodology to automate high-level synthesis of the analog part within mixed-signal ASICs *(Fig. 2)*. An architecture is generated from an analog behavior-

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al description, and a full set of specifications is determined for all of the modules within that architecture.

The ideal flow for a mixed analog-digital ASIC includes high-level specification, high-level design, synthesis, and layout. During specification, the complete ASIC's functionality should be described in a formal way, independent of implementation. The next step is the design of a high-level architecture, including the partitioning into digital, digital-signal-processing, and analog parts. The three parts are then synthesized separately with dedicated tools. When all three parts work, the layout is generated.

Hierarchy must be used to master the complexity of designing a mixed-signal chip. However, major differences exist between the hierarchies used in the digital and in the analog domain *(Fig. 3)*. In the digital domain, hierarchical levels are well defined, and correspond to different levels of signal abstraction. In the analog domain, hierarchies are less strictly defined, and certainly not generally accepted. The levels aren't based on signal abstraction, but rather on a structural decomposition over different levels.

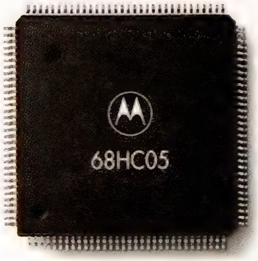
Both commercial and academic tools cover parts of the top-down design flow for the analog subchip. Some tools try to automate the synthesis of analog modules, like analog-to-digital converters (ADCs) or analog filters. And for some mixed-signal ASICs, this may well be sufficient. But no single tool completely automates the synthesis of analog circuitry.

The authors refer to transitioning from the analog subchip to the modules that the subchip is composed of as high-level analog synthesis. Today, this step is performed manually by the designer. A hierarchical structural refinement methodology is the best way to travel through the top-down design of the analog subchip. At each hierarchical level (subchip, module, circuit, device), a synthesis routine for the block under design is executed. Such a routine always consists of the same three tasks: architecture generation, specification translation, and verification.

Mixed-signal EDA is a topic that's carried over into Session 21, which focuses on mixed-signal simulation and behavioral modeling. It's difficult to properly compare the effectiveness of competing mixed-signal simulators, and identify their strengths and weaknesses.

TABLE 1: BENCHMARK TEST CIRCUITS

Circuit names	Circuit function	Number of elements	Number of logic gates
MT1	Clock generator	7	2
MT2	1-bit SRAM	18	4
MT3	biCMOS NAND2	13	1
MT4	biCMOS D-type flip-flop	37	16
MT5	CMOS multiplexer-integrator	9	2
MT6	CMOS shift register	5	1



The Chip.

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A paper written jointly by the University of Illinois, Urbana; National Central University, Taiwan; and Duke University, Durham, N.C., presents the first set of benchmark circuits to evaluate and probe various mixed-mode simulator characteristics. The set of benchmarks consists of six small circuits that test the classical problems in mixed-mode simulation, and four large circuits that represent the target application areas for mixed-mode simulation. Three mainstream technologies—CMOS, bipolar, and biCMOS—are included. Results from transistor-level Spice simulation are used as a basis for the evaluation.

It's difficult to derive a complete set of benchmark circuits to thoroughly test all aspects of mixed-signal simulation. This set isn't exhaustive, but instead represents the types of problems that such a tool must be able to handle. It's intended as a starting point.

TABLE 2: BENCHMARK APPLICATION CIRCUITS

Circuit names	Circuit function	Number of transistors	Number of nodes	% of transistors that are digital
MA205	Digital phase-locked loop	205	124	54
MA445	Bipolar ADC	445	392	75
MA7698	1-kbit SRAM	7,698	3,932	68
MA11591	2-step flash ADC	11,591	5,866	31

A number of important issues, such as signal mapping, local and global feedback, X-state handling, and time-step control, are addressed using a number of small test circuits. Target applications, including memory circuits, phase-locked loops, ADCs, and DACs, are used to assess the speed, accuracy, and modeling capability of the various simulators.

The six test circuits primarily focus on determining the accuracy of mixed-mode simulation as compared to electrical simulation *(Table 1)*. The set consists of a clock generator, biCMOS NAND gate, memory cell, biCMOS D-type flip-flop, CMOS multiplexer-integrator, and a CMOS shift register.

The four larger application circuits, which include a digital phase locked loop, a 1-kbit SRAM, a bipolar ADC, and a MOS ADC, clearly push the limits of Spice's capabilities *(Table 2)*. These benchmarks are meant to determine the overall simulation speed while producing the correct results. Such circuits will give prospective mixed-mode simulator customers a general idea of just how well each simulator performs on actual designs.

MANUFACTURABILITY

Because successfully building newly-designed ICs is always an important issue for engineers, Session 13 offers a group of papers describing the latest in statistical and yield

The Brawn.

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modeling. The increasingly competitive semiconductor market demands that vendors deliver the lowest-cost product possible. Controlling costs, however, requires insight into how design decisions affect the manufacturing cost of an IC.

The Dept. of Electrical and Computer Engineering at Carnegie-Mellon University, Pittsburgh, Pa., produced a paper describing Mapex, their CAD manufacturability analysis environment. Mapex (manufacturability parameters extraction environment), a set of analysis tools assembled in the form of a CAD framework, can extract a large number of design attributes from an IC layout that are relevant to manufacturability and/or yield. The extracted attributes can then be used to improve design tools and strategies, or analyze the reasons for observed loss.

Because extraction is hierarchical, users can examine design attributes of a circuit's low-level partitions that use a specific design tool or library, or those of higher-level partitions where a combination of tools, libraries, and styles are employed. A data-manipulation tool called D-View helps users view and analyze relationships between the extracted physical and structural data. With D-View, users can call up data from the Mapex database to view correlations, regression curves, and confidence intervals. The data can stand alone, or can be manipulated with equations.

Physical design considerations are the topic of Session 24, which covers physical design analysis and optimization. A paper from the Dept. of Electronics, Kyoto University, Japan, proposes a new IC-compaction scheme with shape optimization. The scheme optimizes shapes only for the layout elements on a critical path. The layout is compacted step by step while optimizing the shapes of layout elements. This compaction technique creates layouts that are readily reusable for other sets of device parameters.

Many compaction problems occur in analog layout because elements like transistors, capacitors, and registers have varying shapes. For example, a wide-width MOSFET can form into many different shapes by changing the number of gate folds. Therefore, it's important to determine the most suitable shape for each layout element to produce a compact IC.

The paper outlines a layout technique based on a one-dimensional compaction that uses constraint graphs to optimize shapes only for the elements on a critical path. The shape of one layout element is replaced with a better one in a single process, and the process is repeated until no more replacement is possible. Thus, the layout is compacted step-by-step, while the shapes of layout elements are being optimized.

Another important facet to this compaction scheme is that it allows layout to be reused for other sets of

The Brains.

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device parameters, such as transistor width and length. Generally, the reusability of a fixed analog layout is very low. When a different set of performance specifications is given, it's often necessary to modify device parameters to meet the new specifications, which requires that the layout also be modified.

The technique assumes that a layout has two parts: layout elements that have one or more shape possibilities, and the wires that connect layout elements. Layout elements could be transistors or capacitors, or a set of geometrical figures that represent physical mask patterns and terminal areas to be connected to wires.

A set of blocks on a critical path determine the width of the layout. Therefore, the compaction technique can reduce the width by replacing an element on the path with another shape of smaller width. The height of the overall layout will remain unchanged if the increase in height of the new element is less than the available amount of slack. To sum up, the processing flow of the proposed method consists of four steps: making constraint graphs, selecting the layout element, changing the element's shape, and relocating all elements and wires.

Session 28 unveils work that's been done in physical design for advanced technologies, such as multichip modules (MCMs). Routing thick-film MCMs is distinctly different from pc-board and IC routing. That's because of its three-dimensional makeup, which is due to the large number of layers used (up to 63). The routing process also is complicated by the large number of nets and the considerable grid size. In addition, there are usually many performance constraints for MCM design.

A paper delivered by the Dept. of Computer Science at Western Michigan University, Kalamazoo, Mich., presents a routing methodology that can satisfy a host of performance constraints emerging in thick-film multichip-module (MCM) design. The proposed approach is based on recursively decomposing a complex MCM routing problem into several smaller "tower routing" problems.

All existing MCM-routing approaches, which are extensions of VLSI or pc-board tools, iteratively route either one layer or two adjacent layers. Although this approach is time- and space-efficient, it gives little attention to the performance constraints that dominate thick-film MCM design.

The paper details a completely new routing methodology. Rather than converting the 3D routing problem into a set of 2D routing problems, the new approach decomposes 3D routing into several smaller 3D routing problems. The approach is inherently parallel and incorporates several different performance constraints.

Due to the complexity of routing in the entire 3D space, the routing is complete in several phases. First, tiling partitions the MCM substrate into a set of tiles. The routing space atop each tile is called a tower. The surfaces of a tower are called faces.

Nets are distributed in all three dimensions in a uniform fashion to avoid over-congested towers. Routing distribution ensures that each tower-routing problem is independent. Then routing is carried out in each tower, adhering to performance constraints.☐

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Programmable logic, high-speed signal processing highlight the CICC

User configurability, speedy image and communications signal processors, and low-power CMOS show their potential. **BY DAVE BURSKY**

Digital technologies unveiled at this year's Custom Integrated Circuits Conference (CICC) are dominated by the use and design of user-configurable circuits, image and signal processing, and low-power CMOS processes. The in-system reconfigurability of some field-programmable gate arrays (FPGAs) is opening up new approaches to everything from artificial neural networks to configurable finite-impulse-response (FIR) filters.

Higher levels of integration are adding to FPGA densities as well as to the gate counts of other digital chips like image processors. Such devices must achieve throughputs of over 1 gigaoperation/s to perform real-time image manipulations. Furthermore, the momentum of personal-computing and communications industries has swung lots of attention toward the development of extremely low-power CMOS circuits to help extend the number of useful operating hours a computer or telephone can deliver.

Overlaying custom designs in FPGAs gives designers a great deal of flexibility when it comes to prototyping and testing ideas. In papers from a number of universities in Session 5, reprogrammable RAM-based and one-time-programmable antifuse-based FPGAs were put to the task of implementing an artificial neural network, an FIR filter, and a floating-point coprocessor.

A run-time reconfigurable artificial neural network, developed at the Department of Electrical and Computer Engineering of Brigham Young University, Provo, Utah, can achieve a 500% boost in the number of available neurons without increasing the hardware fivefold. To do that, the researchers took advantage of the RAM-based FPGA, in-system reconfigurability to reuse the hardware. The neural-net algorithm

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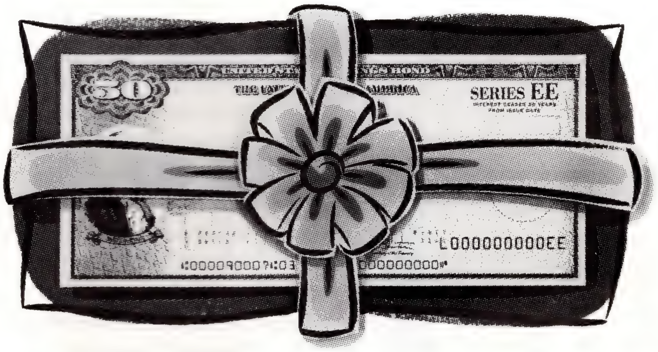
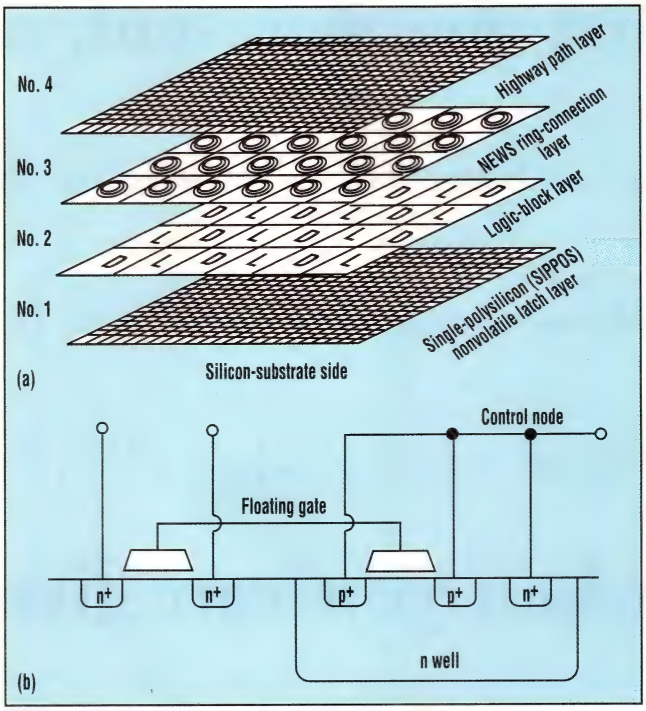


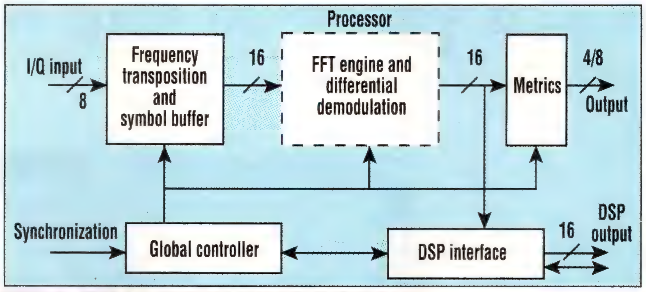
thinks it has many more functions available to it than really exist in hardware. Part of the trick involved dividing the back-propagation algorithm into three sequentially executed stages and configuring the FPGAs to execute only one stage at a time (ELECTRONIC DESIGN, *Apr. 18, p. 40)*.



1. ELECTRICALLY AND LOGICALLY, this four-layer structure (though not a true physical representation) illustrates the implementation levels of a hierarchical EEPROM-based FPGA developed by IBM in Japan (a). At the lowest level are the very simple single-polysilicon pure CMOS EEPROM cells (b). Next are the logic block cells and the local logic interconnection layer that provides north, east, west, and south connections. At the top is the more global interconnect for cross-chip routing.

Reprogrammable FIR filters were the goal of a project undertaken by researchers at the Department of Applied Electronics in Lund University, Lund, Sweden. They employed a pipelined architecture in a Xilinx XC3090 FPGA to form a bit-serial multiplier that executes canonic-signed-digit (CSD) coding. Such an FIR filter can be as complex as a 16-bit, 31-tap Hilbert transformer with eight concurrent multipliers. With the XC3090's input clock set at 20 MHz, this filter can perform 10 million multiplications/s plus many additions, which outstrips the performance of some dedicated commercial DSP chips.

Researchers in the Department of Computer Science at the University of Utah, Salt Lake City, opted to use finer-grain antifuse FPGAs developed by Actel. They prototyped a self-timed floating-point coprocessor that performs IEEE-compatible single-precision computations. The researchers used a pair of Actel 1280 FPGAs, a smaller FPGA (1020A) for some control logic, and a small 15,000-transistor semicustom CMOS chip. With additional circuit improvements, the architecture's self-timed nature shows lots of promise for implementing viable clock-free systems that won't use the synchronous high-speed clocks employed by today's circuits.



2. REAL-TIME ORTHOGONAL frequency-division multiplexing (OFDM) is performed by this IC developed at the Philips Research Laboratories. The signal processor, one of the first chips to execute OFDM, recovers digital-audio broadcast signals. Included on the chip are 160 kbits of DRAM-based buffer memory and a FFT engine that does 8-bit complex computations and performs differential demodulation.

One of the 1280s contains the interface circuits, control modules, and rounding logic, which occupy about 93% of the chip's logic and 69% of the I/O resources. The other FPGA contains the multiplier/divider data path and uses 100% of the on-chip logic yet only 42% of the I/O lines. The CMOS semicustom chip includes the adder, which unpacks the numbers, aligns the mantissa, adds the numbers, normalizes the value, and then rounds and packs the result. The resulting performance of the floating-point unit—about 20 kFLOPS for multiplications and 15.4 kFLOPS for divisions.

The reconfigurability of RAM-based architectures is a key point for system designers that want to alter the system function during system operation or just upgrade the system capabilities. However, the desire to have the same flexibility is also voiced by circuit-board designers. Rather than throw away prefabricated pc boards, Aptix Corp., San Jose, Calif., in Session 9 proposes a new programmable-interconnect structure. It can be employed on circuit boards to provide reconfigurable incerconnections either between the components or as part of a programmable "substrate."

Referred to as FPIC2 (field-programmable interconnect chip, second generation), the chip's internal array structure takes advantage of a new decoded-RAM storage scheme and five-transistor RAM cells. Together, the improvements result in a chip that's 40% smaller than the previous generation with propagation delays reduced by at least 50%. However, the chip functions just like the original interconnection array, which provides a 32-by-32 grid of I/O lines (1024 connections). In addition, the new structure reduces the programming time by almost a factor of 40 (to just 1 ms) over the first-generation chip.

Aptix's designers were able to accomplish all of this with a simpler process than was used for their previous chip. They used the same 0.8-μm design features, except for a double-level metal interconnect structure that was employed in place of the triple-level metal process found in the first-generation device. Furthermore, the new array includes 256 additional buffers so that a path between pins can be

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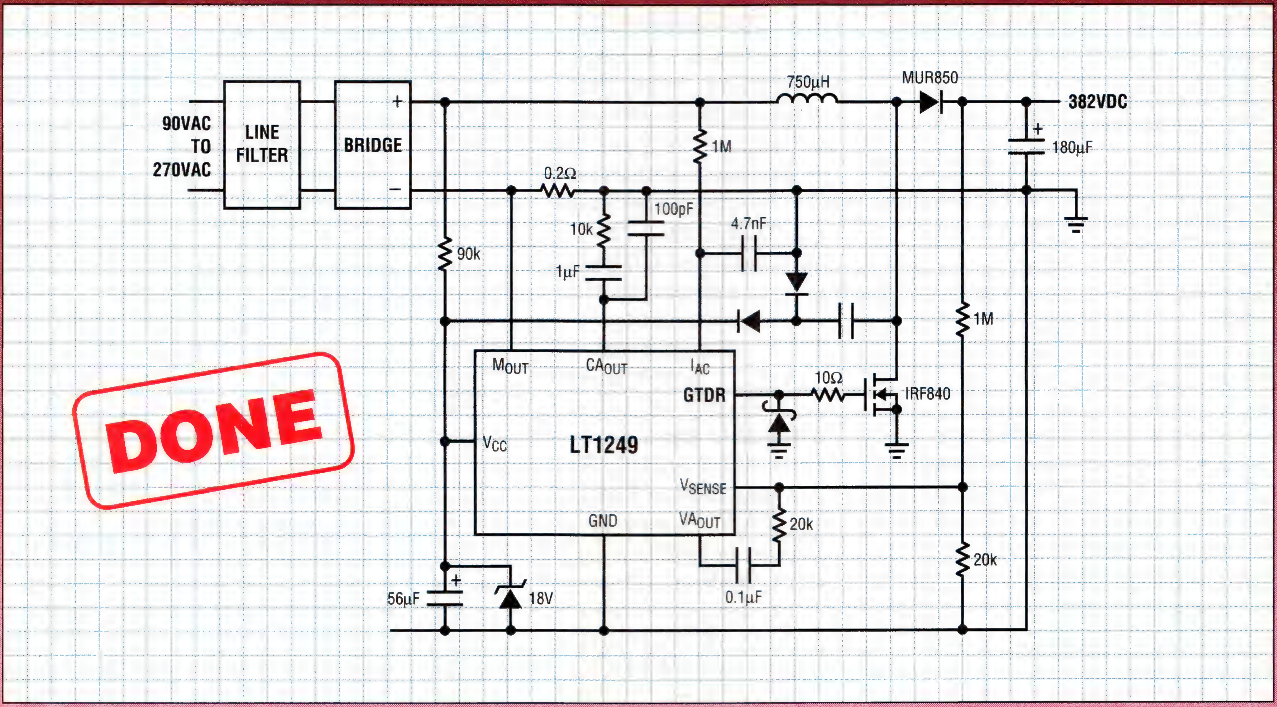

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passive or driven by a buffer for applications that have high fan-out needs. The novel decoding scheme in the FPIC2 chip saves memory by sharing RAM among switch cells, reducing the amount of RAM (and thus chip area) needed. The simpler 5-T RAM cell is more compact than the 9-T cells used in the first-generation FPIC because it only employs a single read/write path rather than separate read and write ports. That also goes a long way toward reducing chip area.

Experimenting with EEPROM storage cells in an FPGA architecture, designers in the Advanced Systems Development Group at IBM, Shiga-ken, Japan, developed a nonvolatile but reprogrammable configuration scheme. The approach uses a hierarchical north, east, west, and south (NEWS) ring interconnection and a highway path that together minimize the number of transfer gates in any signal path *(Fig. 1a)*. That connection scheme is combined with a single-polysilicon pure CMOS (SIPPOS) EEPROM cell that keeps the process simple, minimizing the manufacturing complexity and cost *(Fig. 1b)*.

The FPGA's architecture is hierarchically organized as four "layers." These layers aren't necessarily physical, but are electrical or logical. At the bottom of the hierarchy is the nonvolatile latch layer, which holds the programming data and controls the circuits in the other three layers. The next layer is the logic-block layer, which contains the lookup table circuits and D-type latches. The third layer, the NEWS ring-interconnection layer, enables the logic block's terminal interconnection to go in any direction and allows almost 100% routing of random logic macros. The last layer is the highway path, which provides the long-line routing among logic macros with segmented lines.

In their efforts to find ways to improve FPGA performance, researchers in the Department of Electrical and Computer Engineering at the University of Toronto, Canada, studied various methods of minimizing interconnection delays. They started with the Xilinx FPGAs, exploring techniques to improve the speed/performance by just enhancing the on-chip interconnections. One key contributor to on-chip delays is the segmentation length of the wires. By starting with an analysis of normalized wire segment lengths, researchers noted that the on-chip delays can be decreased by 40% if the unit lengths are quadrupled. Beyond the fourfold increase, longer segment lengths show a slight decrease in performance. Researchers also noted that the efficiency of the routing tools also plays an important role in minimizing delays.

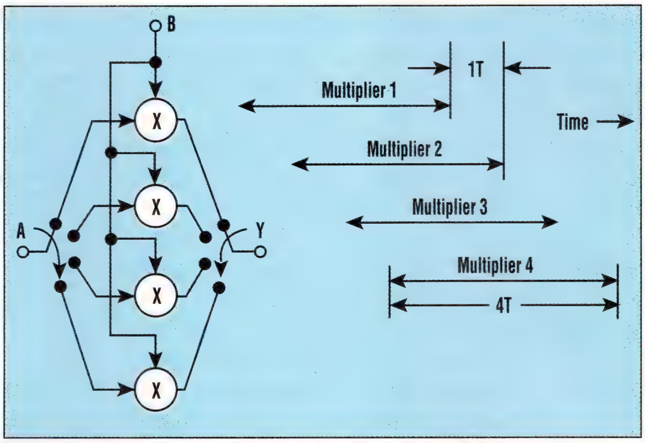
A high-performance EPROM technology is the basis for a high-speed family of high-density programmable logic devices presented jointly by Cypress Semiconductor Corp. and Altera Corp., both in San Jose, Calif. A new process that includes a polysilicon buffer employs locally-oxidized silicon for isolation, and borderless contacts and vias. Using both of these features, along with the new EPROM structure, the designers were able to shrink chip area and trim propagation delays by 50% versus the currently available version of the same device.

With lots of industry focus on low power, designers at Altera also created a dynamically configurable programmable-logic device that can be set to operate at either 3.3 or 5 V. On-chip circuits are dynamically adjusted during post-fabrication testing with power consumption at 3.3 V kept to just 0.5 mW. Both permanent programming for final configuration or temporary reconfiguration for testing is done by opening an on-chip fuse or writing to an on-chip selection register, respectively.

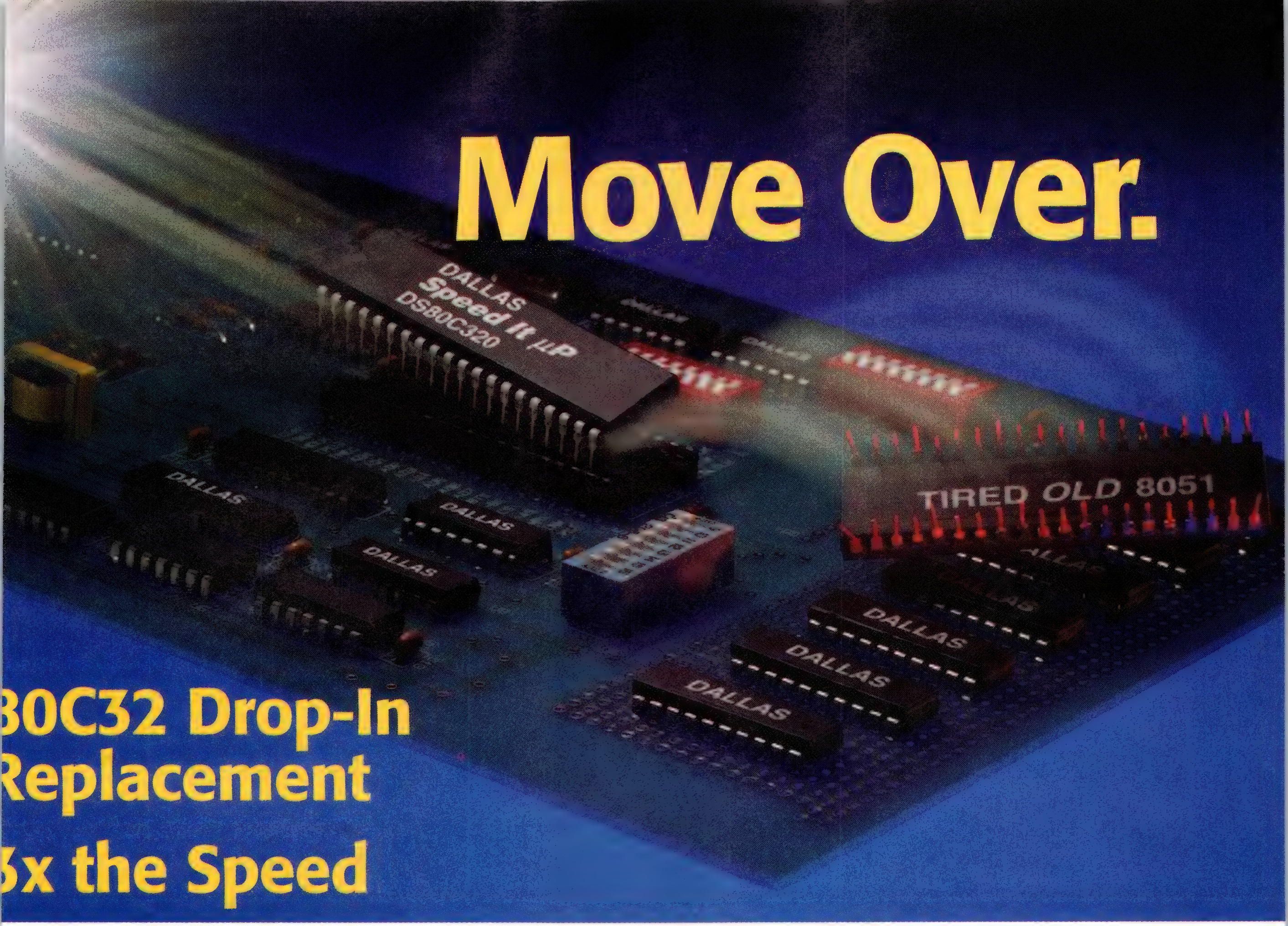
Signal-processing approaches for multimedia, communications systems, and image processing also were high on the list of presentations in Sessions 4 and 6. In Session 4, Philips Research Laboratories, Eindhoven, The Netherlands, describes a demodulator for digital-audio broadcasting. The chip, one of the first to handle the orthogonal frequency-division-multiplexing (OFDM) channel modulation and coding system, supports both terrestrial as well as satellite transmission modes *(Fig. 2)*.

The OFDM chip contains 160 kbits of embedded dynamic memory as well as a complex-arithmetic signal processor that performs the real-time OFDM demodulation. A key feature of OFDM is its ability to do demodulation using a fast Fourier transform (with a radix-2 or radix-4 butterfly), thus making the computations very straightforward. The chip functions on a symbol basis, with each symbol requiring 1.25 ms and containing 4096 samples. The 8-bit input data stream is sampled at 4.096 MHz and combined into 2048 16-bit complex carriers.

After frequency transposition, the complex numbers are buffered in a 2-kword-by-16-bit DRAM bank. Next, a complex 2048-point FFT is calculated on the symbol leading to 1536 carriers. A differential demodulation is applied on the FFT output and the previous symbol, and then stored in another on-chip memory bank. The result is used to generate metrics consisting of one data bit and three reliability bits. In addition to a



3. USING FOUR SUB-MULTIPLIERS staggered in phase by the output period "T" can speed up a 6-bit-by-6-bit multiplication. Not only is this faster than standard 6-bit parallel multipliers, it's also done with lower power drain. The scheme, developed at the University of California at Berkeley, does, however, require more silicon area. Moreover, the overhead associated with the pipeline latches (latch set-up times) decreases the maximum attainable speed.



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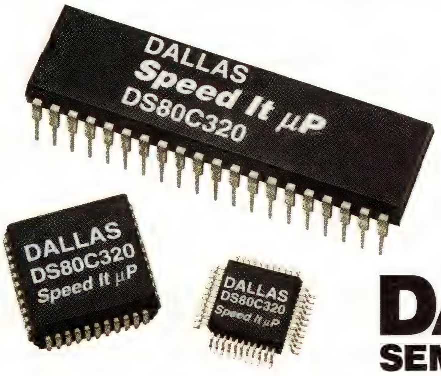

The DS80C320 performs three times faster than other 8051s at the same crystal speed. Running at 25 MHz, the DS80C320 can do six times as much work as a standard 8051.

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4- or 8-bit differential demodulation output, a 16-bit DSP interface is included on the chip for either FFT or differential demodulation outputs.

For high throughput, a 1.2-giginstruction/s image processor developed at the University of Sheffield, Sheffield, United Kingdom, combines both multiple execution pipelines and array processing to handle JPEG, MPEG, and H.261 decompression. The IC has a 16-bit RISC processor to coordinate the chip's activities and a programmable array processor for vector acceleration for image processing at a clock rate of 40 MHz. The programmable array contains 256 1-bit processors, each capable of performing 1-bit addition or subtraction. Every element can communicate through four-way nearest-neighbor connections, and they each incorporate six small addressable RAMs containing a total of 160 bits. The RISC engine acts as a 1D signal processor, while the array of 256 1-bit processor functions as a single-instruction multiple-data engine.

Additional CICC presentations relating to image processing include a data-flow processor first unveiled last year by Array MicroSystems, Colorado Springs, Col., and Samsung Electronics Co., KyungGi-Do, Korea. Others are a real-time object extractor defined by the Image and Media System Laboratory of Hitachi Ltd., Yokohama, Japan, and a real-time classification processor developed jointly by the Universite Montpellier II, Montpellier, France, and the Universite de Bourgogne, Laboratoire G.E.R.E., Le Creusot, France. Voice-band and communications-related signal processors include a variable-length decoding circuit that operates at 162 Mbits/s from NEC Corp., Tokyo, Japan, as well as a multichannel data-compression chip developed by Motorola Inc., Mansfield, Mass.☐

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Speed and smarts pave the way for a new breed of comm chips

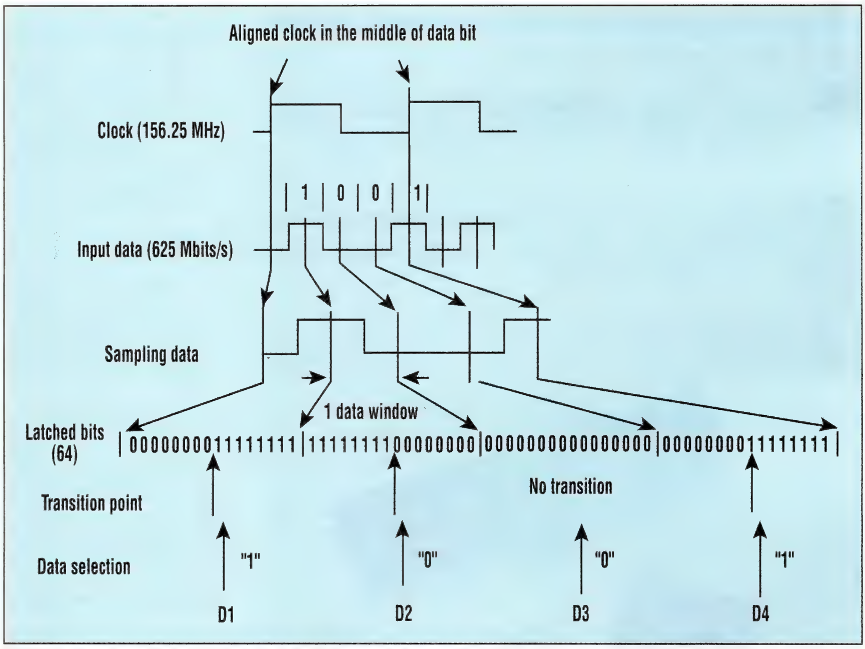
High-speed technologies and new signal-processing techniques produce communications solutions that aren't simply brute force.

BY LEE GOLDBERG

The inevitable quest for faster and more sophisticated communications will receive a boost from an array of new IC developments described at this year's CICC. Supporting these chip-level innovations are increasingly sophisticated solid-state processes that give chip designers more options as they fashion the next wave of silicon. Improved biCMOS fabrication and lithographic line resolutions approaching 0.5 μm have helped silicon chips achieve gigabit operation. Such speeds were only recently the exclusive domain of gallium-arsenide technology. However, GaAs technology isn't standing still either. Prices of GaAs chips are falling while their levels of integration are on the rise, paving the way for cost-effective, double-digit, gigabit-speed GaAs logic.

Over twenty communications-related developments covering roughly three broad categories—data transmission, digital signal processing (DSP), and wireless/RF technologies—were presented at the CICC. In all of these areas, innovative thinking is pushing the limits of higher speeds, lower power dissipation, and higher levels of integration.

In data communications, efforts are being made to fulfill the bold promises of asynchronous-transfer-mode (ATM) gigabit links for desktop computers. As bit rates increase, transmitters and receivers must deal with issues that were not great con-



1. HIGH-SPEED DATA RECOVERY is achieved using a dual-phase, low-speed clock to create a sample window for incoming data. The technique, devised by North Carolina State University, uses a fractional-rate recovery clock that permits a 1:N demultiplexing of data. On-chip delay lines for clock and data reduce phase noise errors.

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PIC16C54A	18	12	512 x 12 (OTP)	25 x 8
PIC16C55	28	20	512 x 12 (OTP)	24 x 8
PIC16C56	18	12	1024 x 12 (OTP)	25 x 8
PIC16C57	28	20	2048 x 12 (OTP)	72 x 8
PIC16CR57A	28	20	2048 x 12 (ROM)	72 x 8
PIC16C58A	18	12	2048 x 12 (OTP)	73 x 8

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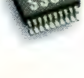

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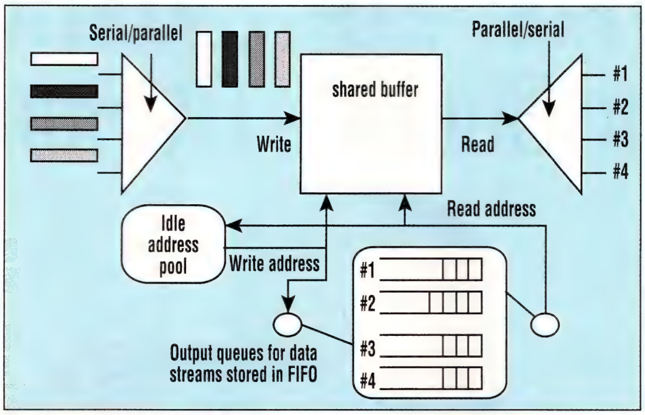
cerns until bit streams began to resemble RF lines. Simply generating or recovering stable, low-noise data at multigigabit rates poses a significant challenge.

A novel data-recovery technique, developed by researchers at North Carolina State University, Raleigh, could provide very stable data framing at high transfer rates. It involves a monolithic data-recovery IC, manufactured in 1.2-μm CMOS, that operates at 625 Mbits/s. This method involves propagating the data and a low-speed (1/4 data rate or less) sampling clock signal through two separate delay taps within the chip. The result is a sampling resolution that's primarily limited by the delay difference between the data and clock *(Fig. 1)*.



2. A SHARED-BUFFER ATM switch, from Mitsubishi reduces buffer memory requirements by using a single common RAM for all channels. An idle-address-pool table locates free-memory space and generates a write address. A dedicated FIFO keeps track of the next byte's location in the queue for each data stream and issues read addresses for the buffer.

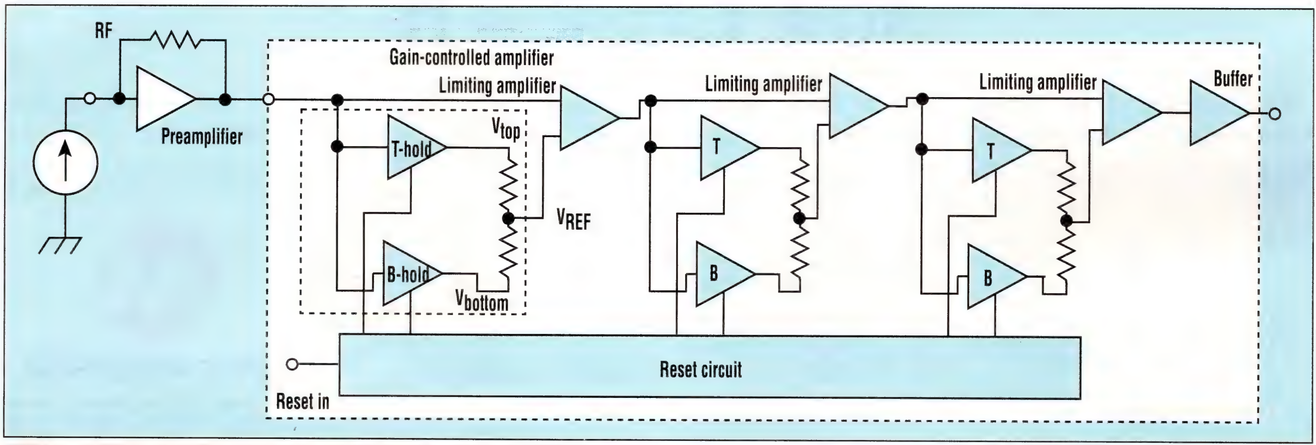
For this super-fast device to operate reliably, phase error must be minimized. Passing both the data and clock through on-chip delay lines helps protect the chip against the two primary sources of phase errors—changes in operating temperature, and fabrication-process variations. A proof-of-concept test article, now being fabricated, will take a high-speed data stream and perform a 4:1 demultiplexing operation. Although the test chip will be implemented in a simple 1.2-μm CMOS process, it's anticipated that operation at 625 Mbits/s will be possible. If successful, this recovery method is easily adaptable to higher-speed device processes.

On the other end of the pipeline, a new solution to high-speed data generation was examined by Hewlett-Packard Co., Santa Rosa, Calif. Using an approach analogous to the recovery circuit previously described, HP designed a 20-Gbit/s 2:1 data selector. The device takes two 10-Mbit/s data streams and creates a single 20-Mbit/s output. The test device was fabricated in the company's GaAs process called HP P-HEMT, which was originally designed for analog microwave devices.

During operation, two 10-Mbit/s data streams are offset in time from each other by a one-half bit-period and fed into the selector along with a 10-GHz clock, resulting in a 20-Mbit/s output. Though it's not a highly-integrated part, the selector is an important building block for future advanced functions.

End-to-end data links also are getting their due at CICC. For example, researchers at Ericsson Radar Electronics, Moldal, Sweden, along with researchers at Motorola Semiconductor, Mesa, Ariz., came up with a silicon bipolar chip set for Sonet/SDH 10-Gbit/s fiber-optic links. The chip set, which acts as a 2.5-Gbit/s data link, uses cascaded high-speed 2:1 multiplexers and demultiplexers implemented in Ericsson's MOSAIC5 bipolar technology. By cascading the multiplexer/demultiplexer circuits, each side of the data link is broken down by a factor of 8:1 to provide eight, 1.125-Gbit/s channels. Although somewhat power-hungry, a preproduction version of a 1:2/2:1 link has been tested at up to 14 GHz with good results.

Another approach to high-speed data links is taken by researchers at the VLSI R&D Center of Oki Electric Industry Co., Tokyo, Japan. Oki's low-power parallel transmitter/receiver ICs are designed for 2.4-Gbit/s optical links. Aimed at short-haul (under 100 m) connections between high-speed data switching and processing equipment, the link employs 11 parallel 320-Mbit/s channels that run through a single 12-core, multimode, optical fiber tape. This approach was selected to take advantage of cost and power savings de-



3. THIS HIGH-SPEED OPTICAL RECEIVER created by NTT uses a feedforward system to control gain and bias. The configuration eliminates the need for external passive filter elements and reduces volume and parts count.

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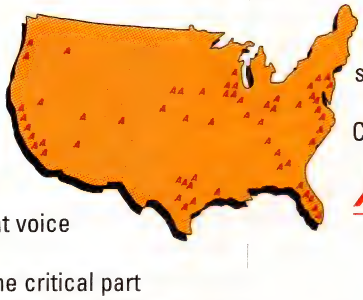

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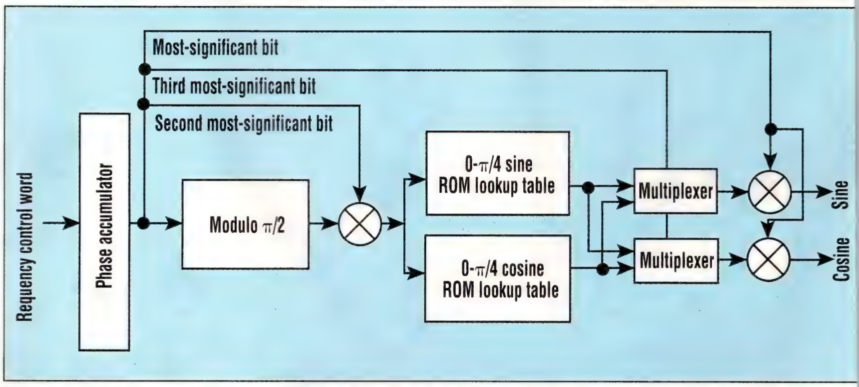
Most-significant bit
Third most-significant bit
Second most-significant bit
Requency control word
Phase accumulator
Modulo π/2
0-π/4 sine ROM lookup table
0-π/4 cosine ROM lookup table
Multiplexer
Multiplexer
Sine
Cosine

4. THIS 200-MHz SYNTHESIZER/MIXER uses compressed sine/cosine lookup tables to produce low-distortion waveforms. It was proposed jointly by Broadband Telecom and the University of California at Los Angeles.

rived from using medium-speed, low-power bipolar technology in the transmit and receive stages.

As ATM networks and switch fabrics become more complex, efficient means of providing data buffering must be found. In most conventional switch designs, each channel has its own buffer FIFO, which by necessity must be as large as the maximum predicted data backlog for any given channel. When implementing a switch of any significant complexity, the combined memory requirements rapidly outgrow the capacity of one chip, even though most of the memory is not used simultaneously.

One approach that makes more efficient use of switch-element buffer memory employs a common RAM shared by all channels. Proposed by scientists at Mitsubishi Electric System's Laboratories in Itami and Kamakura, Japan, the switch structure uses a dedicated FIFO with a search circuit that assigns the common memory's next available portion to incoming ATM cells. It does this while keeping track of its location for withdrawal from the buffer in the proper sequence *(Fig. 2)*. A separate idle-address-pool table keeps track of available memory within the buffer as cells come and go. This architecture significantly reduces memory requirements for switch elements, making on-chip buffers feasible for many applications. A 0.5-μm CMOS evaluation chip was fabricated, and it achieved an interstage transfer speed of more than 500 MHz and a cycle time of over 125 MHz.

Another 0.5-μm process is proposed for a gate-array chip that will find use as a user-network interface for the 622-Mbit/s B-ISDN. However, it's a low-power biCMOS process. The single-chip device, proposed by researchers at the Mitsubishi System LSI Laboratory, Hyogo, Japan, is being designed to provide interfaces between workstations and high-speed communications devices. The biCMOS process with which it's made permits CMOS, TTL, and ECL devices to be incorporated on the same chip. This would free designers to implement only the highest-speed sections of the circuit using power-hungry bipolar transistors. The remaining sections would be in CMOS, thus reducing power requirements significantly while retaining the 622-Mbit/s throughput.

DENSER RF ICs

The increasing demand for wireless consumer electronics has prompted researchers to push the limits of IC technology in several directions at once. In the rough-and-tumble consumer electronics market, engineers face constant pressure to make their products smaller, more sophisticated, and less expensive. Meeting these seemingly divergent goals requires IC designers to adopt a multi-pronged strategy: Integrate more functions on a chip, add programmability wherever possible, and squeeze power consumption (i.e. battery size) down to a minimum.

This is exemplified in the receiver IC developed by the design team at NTT LSI Laboratories, Kanagawa, Japan. The CMOS optical receiver uses a feedforward auto-bias adjustment to achieve both wide dynamic range and extremely high sensitivity. Conventional receivers with AGC and automatic offset control circuits typically require external passive components. To eliminate them, the team developed a receiver that employs a multistage, feedforward system to control gain and bias *(Fig. 3)*. The receiver requires no peak-hold capacitors or other external elements.

Reducing component count by substituting digital processing for analog filtering is another growing trend, as shown by engineers from Ashi Kasei Microsystems, San Diego, Calif., and Tokyo, Japan. They developed a low-noise integrated 455-kHz IF stage filter for advanced mobile-phone service (AMPS) cellular-telephone applications. Their design employs multistage, repeating AGC and filter blocks instead of conventional ceramic filters. The first chip to apply this filtering technique demonstrated a dynamic range of 64 dB with a signal-to-(noise + distortion) ratio of 40 dB.

Parts count and power are being further reduced as the modulation and demodulation of signals is migrating to the digital domain. Designers at Siemens A.G., Munich, Germany, describe a single-chip, 60-Mbit/s quadrature-amplitude-modulation (QAM) demodulator. Implemented in 1-μm CMOS, the chip performs all digital baseband processing for QAM, including carrier recovery and adjustment of bias functions in its input ADCs.

Further integration of IF functions through mixed-signal processing was demonstrated in a single-chip implementation of the quadrature phase-shift-keying (QPSK) modulation scheme used in Japan's personal handy phone (PHP). The combined analog/digital modulator chip, developed by Ashi Kasei Microsystems, is implemented in 1.2-μm CMOS. Containing both analog and digital functions, the chip can synthesize and filter a QPSK signal and provide I and Q signals to a 1.9-GHz RF modulator. Both CMOS digital circuits and low-threshold n-channel transistors were used where possible to minimize power use.

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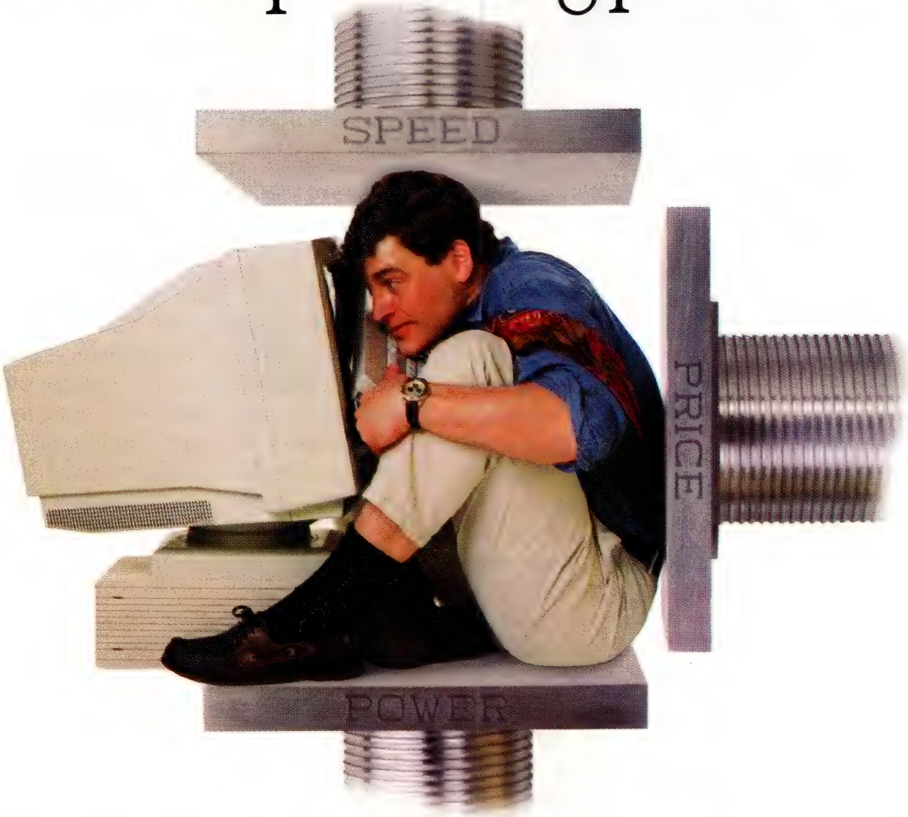

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Slew Rate (V/μsec)	1200	1500	1100	2100
Diff Gain/Phase (%/°)	.01/.025	.02/.025	.02/.02	.12/.05
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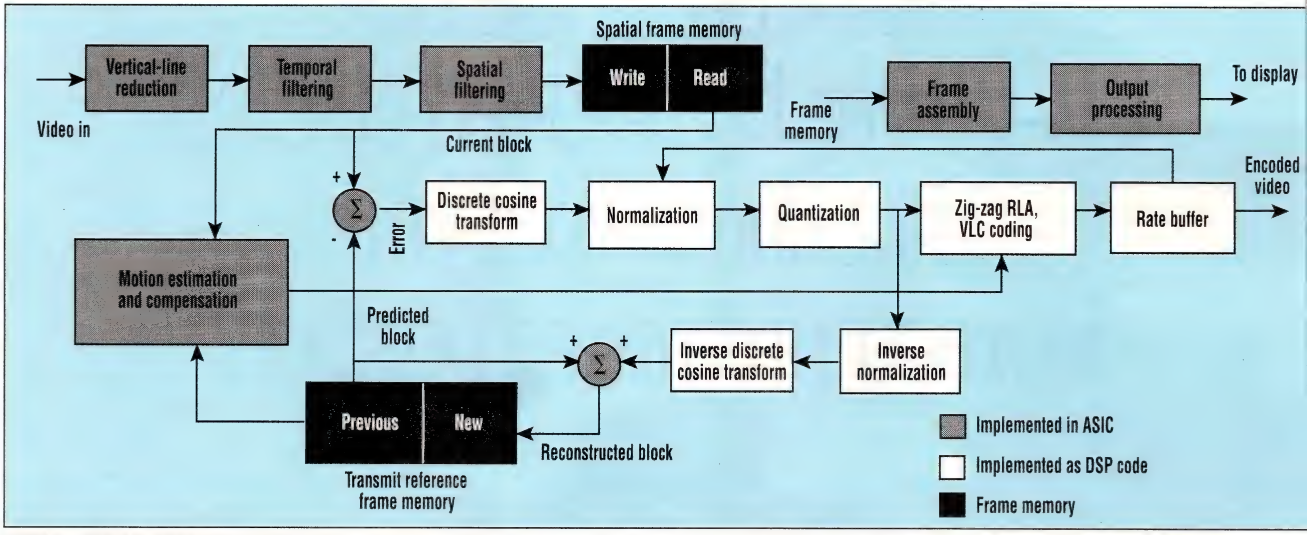

5. THIS VIDEO CODEC reduces appliance-quality video to a 10-kbit/s data stream using discrete cosine transform (DCT) filtering along with intra- and inter-frame motion compensation algorithms. Developed by AT&T Bell Laboratories, it partitions hardware and software between ASICs and DSP code.

bring CMOS switching speeds into the near-gigahertz range. Taking advantage of the watt-pinching performance that CMOS offers, many companies now are producing low-power solutions for wireless applications. A case in point is the all-CMOS, 900-MHz, mobile RF synthesizer developed jointly by Mitel Semiconductor, Kanata, Ontario, Canada, and the Carleton University Department of Electronics, Ottawa, Ontario, Canada. The monolithic synthesizer employs a digitally programmed VCO, and offers –94-dBc/Hz phase-noise performance at 800 to 900 MHz while drawing only 18 mW at 5 V.

CMOS also demonstrates its versatility in the design of a 200-MHz digital synthesizer/mixer developed by Broadband Telecom along with the University of California, both in Los Angeles. The synthesizer is completely digital and uses a pair of sine- and cosine-generation tables for rapid waveform generation *(Fig. 4)*. To save space, only the first quadrature of data is stored in the table, with the remainder of the waveform reconstructed via interpolation. Exploiting the chip's digital nature, the designers add selectable frequency, phase, or quadrature-amplitude-modulation capability. Operating at up to 200 MHz, the chip offers spectral distortion below –84 dBc while drawing 2 W at 5 V.

Low-power technology was put to a novel application in an antenna-powered transponder system developed by Texas Instruments Deutschland, Freising, Germany. The system is intended for use in field applications, ranging from security to livestock management to access control, where a transponder should be rugged, require minimum weight and volume, and remain independent of any external power source. The TI transponder chip gets its power from a burst of RF energy that's periodically emitted by a reader unit. This energy charges a small external storage capacitor and triggers the chip's transmit function. At the end of its RF burst, the reader unit switches to the receive mode while the transceiver chip outputs a digital sequence stored in its EEPROM using frequency-shift-keyed (FSK) modulation over a 134.2-kHz carrier.

DSP AS AN ENABLER

Digital signal processing (DSP) is at the center of today's rapid advances in communications. The complicated compression and noise-cancelling functions found in many communication products are almost exclusively performed in the digital domain. Although processing analog waveforms is often necessary and sometimes more efficient, digital processing offers a high degree of flexibility due to the programmable nature of many DSP ICs. As an example, a fully digital cellular transceiver might some day be able to support AMPS, time-division multiple-access (TDMA), Group Speciale Mobile (GSM), or even code-division multiple-access (CDMA) communications simply by invoking different parts of its embedded software. Several novel applications of DSP technology introduced at CICC may prove significant.

Engineers from Texas Instruments, Dallas, discussed their recently unveiled multimedia video processor, the MVP—an extremely enhanced version of the powerful TMS320 DSP IC. The MVP chip features four independent, fully programmable, 32-bit parallel DSP circuits controlled by an embedded RISC-based controller. The five processors can share their 25, 2-kbyte, on-board RAMs as well as off-chip memory, and support sophisticated image processing with up to two billion operations/s. The on-board video-interface controller can perform frame-grabbing and frame-generation functions under the control of the master processor, using either internal or external data.

Video compression is a hot topic these days, with everybody trying to narrow the bandwidth requirements for applications like desktop video and video telephony. An interesting development in this area is the result of a joint effort between researchers at AT&T Bell laboratories, Allentown, Pa.; C-Cube, Milpitas, Calif.; Compression Labs, San Jose, Calif.;

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Crystal Semiconductor, Austin, Texas; and TLW, Burlington, Mass. This project produced the prototype of a low-cost codec for consumer video phones. Designed to work with the AT&T DSP1616 processor, the codec performs preprocessing, motion estimation, and compensation for incoming images and reconstructs images from compressed data.

MULTILEVEL COMPRESSION

To reduce a 30-frame/s color image to a 10-kbit data stream, several levels of compression are required *(Fig. 5)*. First, preprocessing is applied to cut the number of lines in half by averaging each pair. Next, temporal filtering is performed to reduce noise and smooth motion. Redundant sections of images then are compressed, and 16-by-16 blocks are compared to the previous frame by a dedicated "motion estimation engine" to identify those parts of the image that change from frame to frame. By using this backward comparison, the codec can identify the moving portions of the image and transmit a description of the motion rather than the entire image. In this implementation, the tasks are divided between the processor and the codec, with those functions best accomplished in software being executed by the DSP1616 IC. Initial results are promising, with the prototype chip operating at 30 MHz and processing 25 frames/s.

Looking toward the next generation of signal-processing technologies, we can expect to see neural networks begin to find applications in real-world products. An interesting application of a neural network for medical image processing is detailed by the U.S. Department of Defense, Fort Meade, Md., and the U.S. Naval Research Laboratory, Washington D.C. After verifying the approach in software, researchers implemented a 10-by-10 neural-net array in a 2-μm p-well process that would extract features from tomography scan data. The test results showed that the prototype could perform the image processing quickly (0.5 μs) and reconstruct features from simulated scan data with good accuracy. Current IC-fabrication technology will permit construction of a 100-by-100 array that's able to provide real-time imaging for CAT and PET scanners, a real plus for medical diagnostics as well as other industrial applications.

Once neural-net system implementation is better understood, its speed and flexibility holds promise for many applications where the input information is ill-defined or somewhat ambiguous. This includes speech and image recognition, multideterminant control systems, as well as military and civilian radar signal processing.☐

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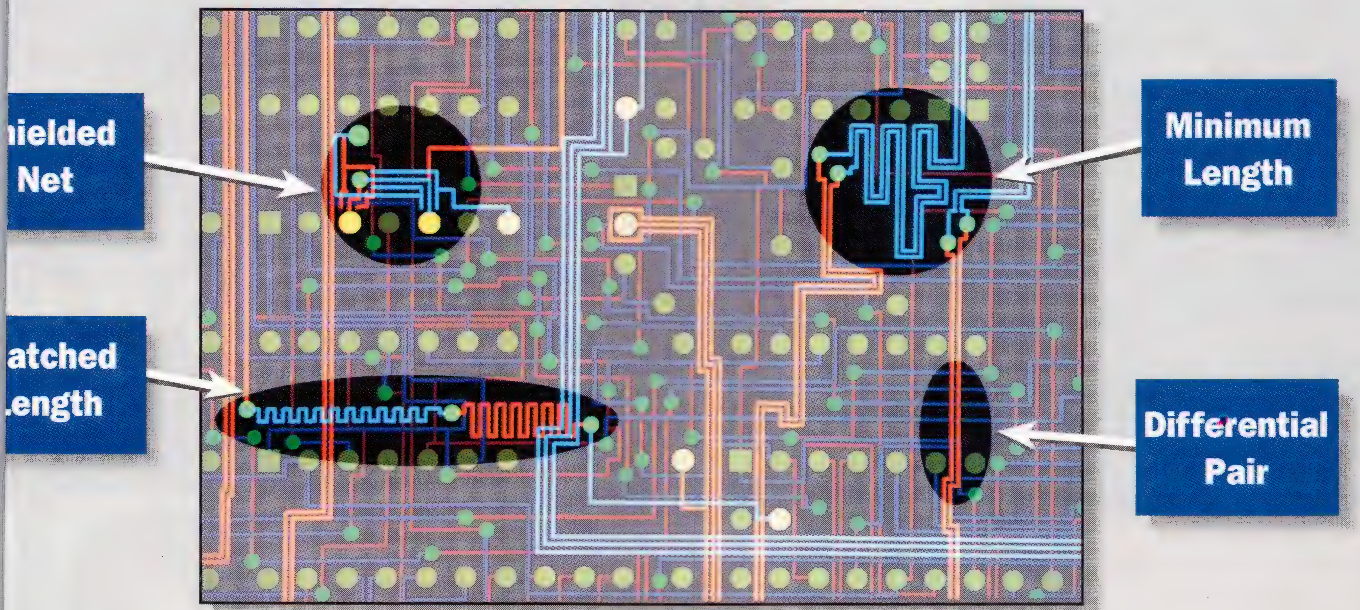

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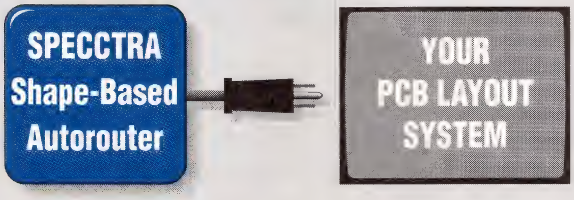

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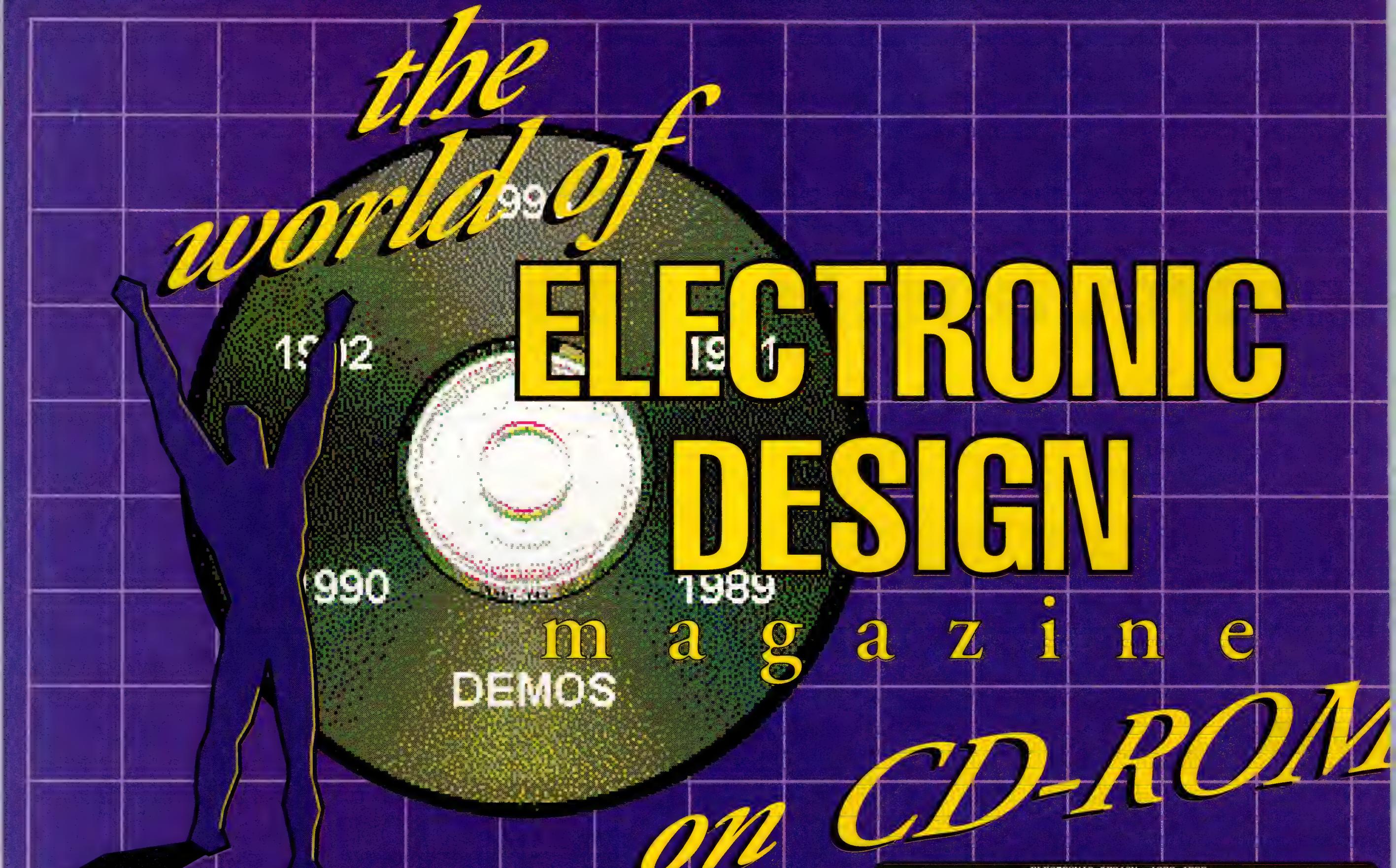

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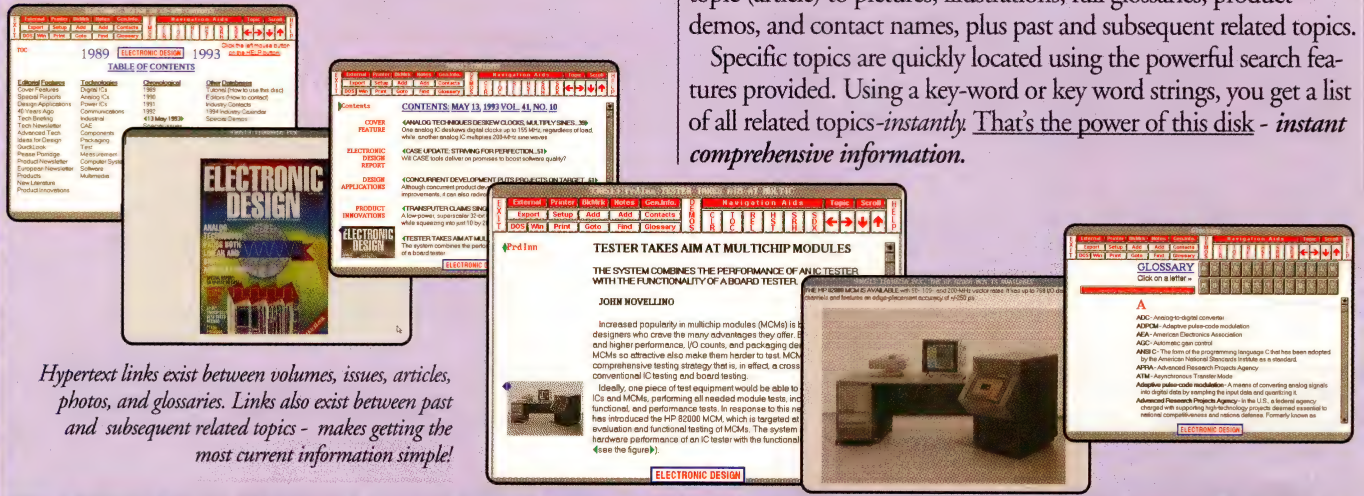

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Click the left mouse button on the HELP button.

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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is b
designers who crave the many advantages they offer. E
and higher performance, I/O counts, and packaging de
MCMs so attractive also make them harder to test. MCM
comprehensive testing strategy that is, in effect, a cross
conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to
ICs and MCMs, performing all needed module tests, inc
functional, and performance tests. In response to this ne
has introduced the HP 82000 MCM, which is targeted at
evaluation and functional testing of MCMs. The system
hardware performance of an IC tester with the functional
(see the figure).

THE HP 82000 MCM IS AVAILABLE with 50-, 100-, and 200-MHz vector rates. It has up to 768 I/O ch
channels and features an edge-placement accuracy of +/-250 ps.

GLOSSARY

Click on a letter »

A

ADC - Analog-to-digital converter

ADPCM - Adaptive pulse-code modulation

AEA - American Electronics Association

AGC - Automatic gain control

ANSI C - The form of the programming language C that has been adopted by the American National Standards Institute as a standard.

APRA - Advanced Research Projects Agency

ATM - Asynchronous Transfer Mode

Adaptive pulse-code modulation - A means of converting analog signals into digital data by sampling the input data and quantizing it.

Advanced Research Projects Agency - In the U.S., a federal agency charged with supporting high-technology projects deemed essential to national competitiveness and national defense. Formerly known as

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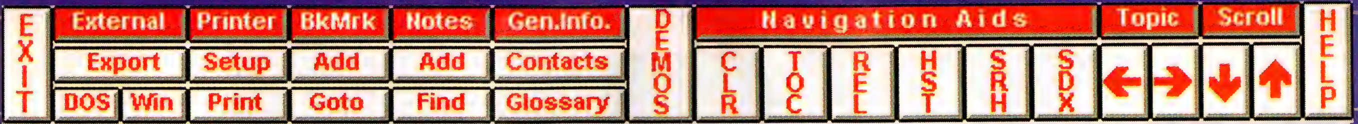

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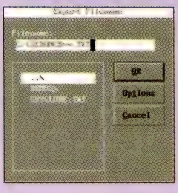
Powerful, hypertext-based commands let you quickly and efficiently find, re-find, link, make notations, leave bookmarks, export, print, search, get product demos, and even return to your operating system!

EXIT - *Leaving so soon?*

The EXIT button quits the application, and takes you right on out into the cold, cruel, computer world. If you want to leave the Electronic Design Magazine, and still have easy access without re-launching, use the **DOS** and **Win** buttons. These are located under **External** *(see below).*

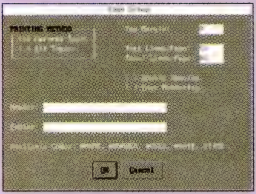
External - *Life beyond this disk*



The **Export** button will export any or all of an article based on your selection.

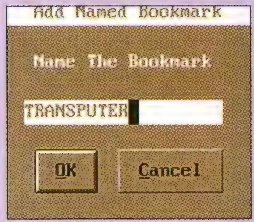
DOS & **Win** - DOS brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. Return to Electronic Design Magazine, where you left off, without re-launching.

Printer Commands



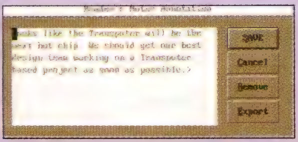
Setup & **Print** - Articles, editorials, glossaries, table of contents, illustrations, and photos (if your printer is capable).

Bookmarks and Notes - *Leaving your mark*



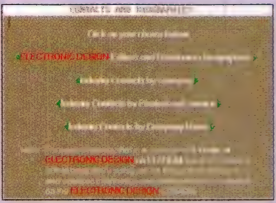
BkMrk - Bookmarks flag topics for future reference, just like using a bookmark in a real magazine. You mark a spot, and the bookmark is stored even if you quit. **GOTO** brings you back to your bookmarks. Deleting them is just as simple.

Notes - Add and find your own notations. Notes stay until you delete them, even after you quit.



Looks like the Transputer will be the next hot chip. We should get our best design team working on a Transputer based project as soon as possible.

Gen. Info - *Complete reference and more!*



Contacts are complete with company and contact names, phone numbers, and addresses. All of the information you'll need to follow up.

Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

DEMOS - *Instant products demos and information*

This button gives you pertinent product demos and information. Submitted by the manufacturer, demos often include live action footage, most in color.

Navigation Aids - *Magellan you're not, and you don't need to be*

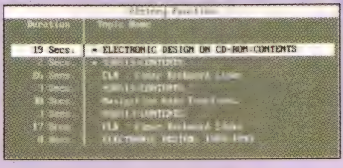
All the aids you'll need to motor your way through this CD in no time flat.

CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

TOC - *Table of Contents* - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.

REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.



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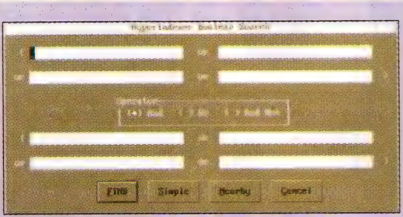

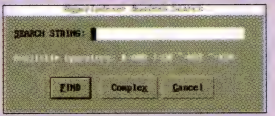

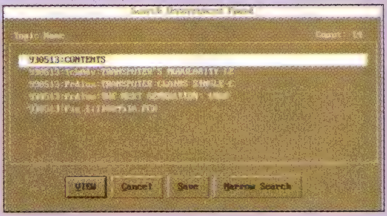

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SRH - *Search* - Conduct simple, complex or proximity indexed searches.

SDX - *Subject Index* - A hierarchical list of key subject areas compiled by the Editors of Electronic Design. The index also allows direct access to related topics.

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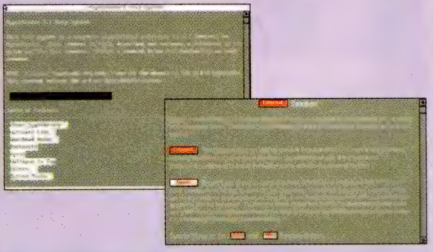

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ELECTRO 94 TARGETS THE WORLDWIDE MARKET

SESSIONS ON GLOBAL OPPORTUNITIES AND CHALLENGES HIGHLIGHT AN EXTENSIVE TECHNICAL PROGRAM.

JOHN NOVELLINO

Information on how to be successful in the international marketplace and meet the challenges of today's competitive pressures will form the cornerstone of the conference program at the upcoming Electro International 94. The two issues are among the nine subject tracks to be featured in the program, which includes topics ranging from advanced technology to areas of interest to company CEOs.

The 56 conference sessions are part of a technical program that also includes 14 tutorials and two special workshops on virtual reality (VR). The show will be held May 10 to 12, with the tutorial program beginning on May 9 at the Hynes Convention Center in Boston.

Subject tracks represent such areas as engineering technologies, careers/education, software and standards, networks, and manufacturing. Issues the electronics industry faces in the global marketplace will be the focus of three tracks covering emerging technologies, international business, and purchasing/business. Finally, a track called "executive business," which is aimed at CEOs, entrepreneurs, and senior executives, will discuss global forces and influences expected to affect the industry into the year 2000.

The conference will equip engineering professionals with the tools they need to survive and prosper, according to Edward U. Lee Jr., chairman of Electro 94's board of directors. "To create demand and grow profits are the most important challenges in today's electronics marketplace," says Lee, who is engineering group manager at Digital Equipment Corp.'s Systems Technical Operation. "Engineering-driven profits fueled by products and processes that stimulate demand are the keys to competitive advantage and survival."

Lee emphasizes the international nature of the show. "This year we began a worldwide marketing thrust that focuses on the reengineering issues facing the electronics industry today," he says. "By offering a spec-

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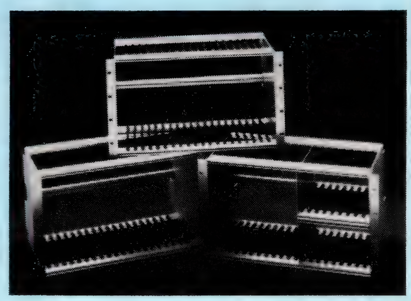

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■ *Booth 5317*

trum of world-class professional programs, progressive solutions, and interactive demonstrations, we empower electronics professionals by giving them the tools to successfully meet today's competitive pressures."

In fact, one entire track of the technical program is devoted to International Business. One session in that track, "Understanding European and International Safety Standards," will discuss product safety issues that must be considered before designers can build prototypes and go into production. Another session, "ISO 9000—Its Effect on Your Company," covers the new international standard for a quality management system. The standard has been adopted by agencies in 59 countries, including the U.S. Department of Defense and the Food and Drug Administration.

The Engineering Technologies track includes a session called "EDA Vendor Support for High-Speed-System Physical Design." The premise of the session is that companies will have to change their design methods to handle the next generation of high-speed systems. EDA vendors, therefore, must come up with more sophisticated tools for the design of these systems, including the physical layout and analysis of boards and multichip modules (MCMs). Representatives of four EDA companies each will describe one technology their firm has identified as critical to supporting this need.

Also under Engineering Technologies, a session called "Concurrent Engineering: Concepts and Practice" focuses on the factors critical to the success of concurrent engineering. These include encouraging functional groups to get along and keeping a project on track through metrics, which the session description calls the most overlooked aspect of concurrent engineering. Presenters will provide insights and lessons learned at several companies.

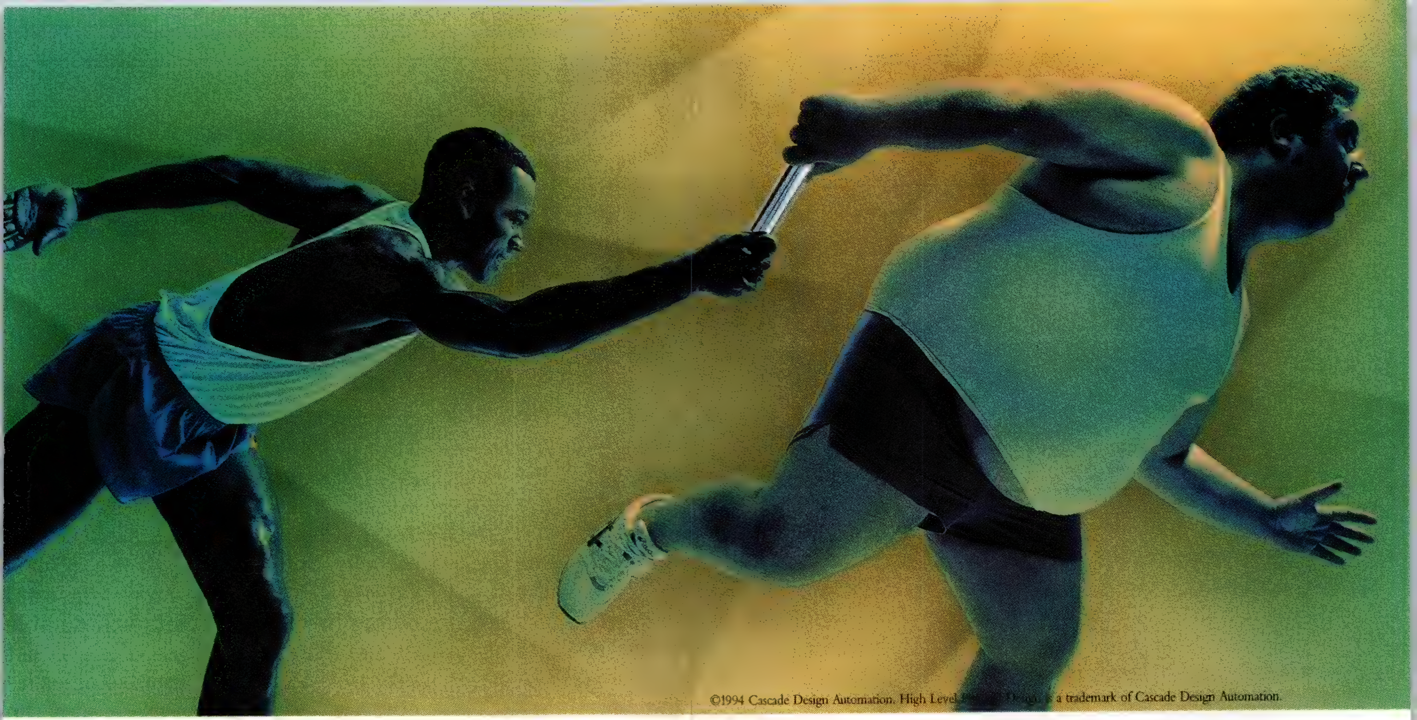
MCMs have been a hot topic in recent years, but problems associated with lack of physical access for testing and high packaging density have slowed their implementation. Three technical sessions at Electro 94 will take on these problems. Although they're part of the Manufacturing Processes track, the sessions deal directly with concerns of design engineers.

The session on "Testability Techniques for Multichip Modules" will cover testability approaches designers can take with MCMs. It will emphasize methods that can be used for bare die, unpopulated substrates, and assembled modules. A session simply titled "MCMs" will alert designers to choices made during the design phase that affect a product's verification and testing phases. The use of certain techniques can even help engineers validate their designs. Finally, a session on "Thermal Management" points out that choices made during the design phase dictate 75% to 80% of the product's manufacturing costs. Speakers will demonstrate how making the right choices on thermal management can result in a more successful product.

The manufacturing track also addresses the difficulty in testing complex circuits in "Using the IEEE-1149.5 Module Test & Maintenance Bus." The recently developed MTM bus, which simplifies the integration, debugging, and testing process, employs a set of predefined commands to access standard functions, including data transfer, testing, and initialization functions. Among the topics to be discussed are an introduction to the bus and how to interface the bus to IEEE-1149.1 boundary-scan circuitry.

The tutorials will be held on the Monday and Thursday of the show week. The wide range of topics run from "Basic Project Management" to "Tools for Strategic Planning." Software, which is a larger part of each succeeding generation of products, will get its share of attention. One tutorial will discuss the "Testing of Object-Oriented Software," while another will take on "Total Software Quality Assurance."

Those looking to make process improvements at their companies will be interested in a tutorial that teaches participants how to apply the principles developed by Genichi Taguchi. The session, called "The Taguchi Method: Designing for Robust Qual-



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READER SERVICE 153

ity," will show how to setup and analyze Taguchi's experimental designs, identify variables that affect process centering and variation, and use the loss function concept to apply unique cost values to products.

The VR workshops, which will be presented by the Virtual Reality Alliance of Students and Professionals, include one on "The PC-Based VR Glove" and one on "PC-Based VR Animation." The glove session will discuss applications of the Mattel Power Glove with IBM personal computers. Participants will be able to use the glove, which is a low-cost alternative for a 3D input. Topics include interfacing the glove and the personal computer, and how to write C and C++ programs that can be used with the glove.☐

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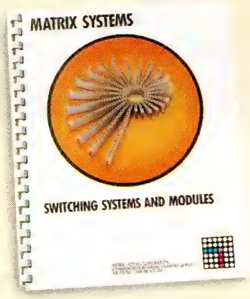

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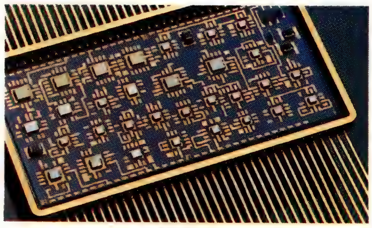

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SUB-30-V POWER DMOSFET TECHNOLOGY BRINGS POWER-MANAGEMENT FET SWITCHES TO SYSTEMS WITH EVER LOWER ON-RESISTANCE.

P-DMOSFET AND TSSOP TURNS ON WITH 2.7 V_{GS}

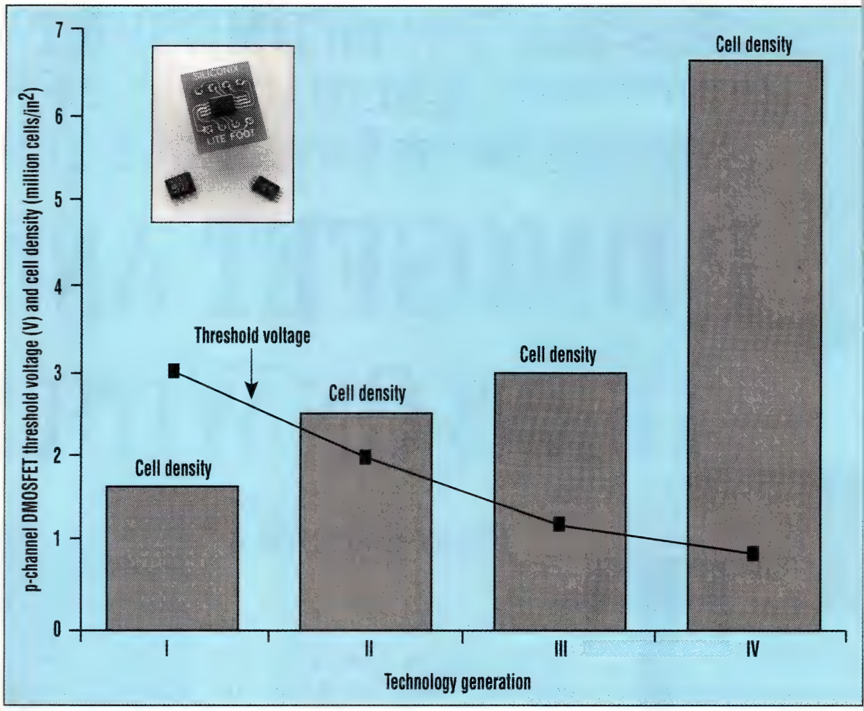
FRANK GOODENOUGH

The demand for greater power efficiency from all kinds of equipment, from battery-powered PCs and instruments to line-powered systems, has promulgated the buzzwords "power management." At the heart of power management, which is the ability to ration power to individual system blocks for short lengths of time ranging from milliseconds to minutes, lies low on-resistance logic-controlled solid-state switches, usually in the form of MOSFETs.

Within the world of MOSFETs, the move to logic levels below 3 V combined with the need for 5 to 10 V of high-side drive in n-channel FETs has precipitated a demand for p-channel devices that can be fully enhanced (turned on hard) with 2.7 V. These switches must take up "zero" pc-board space, have "zero-voltage drop" across them, and dissipate "zero" power while passing current.

Taking those requirements into account, designers at Siliconix combined recent innovations in surface-mount power-IC packaging with fourth-generation low-threshold-voltage p- and n-channel vertical double-diffused MOSFET (DMOSFET) technology. Their achievement, which essentially redefines the performance limits of ultra-miniature power MOSFETs, resulted in a single p-channel MOSFET die, the first in a new family of power MOSFETs dubbed Lite Foot. Called the Si6433DQ, its typical on-resistance runs a mere 70 mΩ, and it needs only 2.7 V between gate and source (2.7 V of gate drive) to reach that on-resistance. Moreover, it comes in a virtually invisible 8-lead TSSOP *(Fig. 1, insert)*. To permit breadboarding, Siliconix provides TSSOPs in sample quantities mounted on the small pc board. In the same family, an equally-sized n-channel FET exhibits a typical on-resistance, $R_{DS(on)}$, of 35 mΩ. Under similar gate drive, the Si6433DQ's maximum $R_{DS(on)}$ is still just 110 mΩ.

To achieve that low $R_{DS(on)}$ in such a small volume, the die and package design were performed in tandem. The package design of Lite Foot was established simply by follow-



1. GREATER CELL DENSITY and voltage scaling have produced four generations of DMOSFETs from Siliconix. Each generation shrinks the die sizes and lowers threshold voltages, ultimately leading to tinier packages. Fourth-generation devices, 35-mΩ p-channel FETs, come in 8-lead TSSOPs (inset).

ing the success of its Little Foot product line (low-voltage, low-$R_{DS(on)}$ power FETs in an SO-8 package). The design maximizes power dissipation without the need for external heat sinking other than the pc board. As a result, it can dissipate over 1.5 W in a tiny 8-lead TSSOP.

Put in perspective, beyond its thermal performance, the $R_{DS(on)}$ offered in the TSSOP with just 2.7 V of gate drive is now less than that available in the SO-8 package with a gate-to-source voltage (V_{gs}) of 4.5 V. Such on-resistance improvements result from the cell density and voltage scaling made possible by fine-line fabrication technology previously used only in high-density ICs. Lite Foot uses a planar DMOS structure that provides densities in excess of 6.7 million cells/in.^{2}. Power MOSFETs are really ICs that consist of large numbers of individual MOS (in this case vertical DMOS) transistors, or cells, all connected in parallel. For p-channel DMOSFETs, this cell density achieves a 5-V specific on-resistance of better than 1.5 mΩ/cm^2.

Other performance numbers for the Lite Foot MOSFETs include maximum drain-source voltage (V_{ds}) of –12 V, maximum V_{gs} of ±8 V, continuous drain current (at 25°C) of ±3.7 A, and pulsed drain current of ±30 A. Transconductance typically is 11 siemens. Maximum turn-on delay, rise time, turn-off delay and fall time run 60, 100, 180, and 100 ns, respectively.

BETTER PMOS DIE

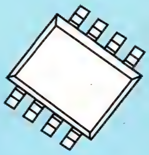
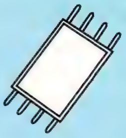
Voltage scaling of vertical DMOS devices (just like scaling the high-density ICs that they are) improves a device's electrical performance by optimizing its characteristics for a specific voltage range. The p-channel DMOS technology initially developed for Lite Foot uses this voltage-scaling principle to drop the rated gate and drain voltages to the lower voltages commonly encountered in battery-powered and low-voltage logic applications. Such voltage scaling has proceeded over four generations of p-channel DMOS technology *(Fig. 1)*.

Each generation of DMOS has achieved a lower threshold voltage (V_t) as a result of its higher cell density. However, each generation requires a tighter tolerance for critical dimensions during patterning and etching, more stringent layer-to-layer registration, and more accurate dopant-profile control.

While the first generation utilized proximity aligners and deep junctions to achieve a density of 1.6 million cells/in.^{2}, the second generation required 1X stepper technology to attain 2.5 million cells/in.^{2}. The fourth generation technology, which achieves 6.7 million cells/in.^{2}, becomes practical only in a Class I wafer-fabrication facility that uses 5X reduction steppers. A portion of a die layout in the third- and fourth-generation technologies, shown to the same scale, indicates rather well the relative cell densities *(Fig. 2)*. In addition to tighter cell spacing, this density demands shallow junctions and submicron channel lengths that previously wasn't used to build power FETs.

Over time, and driven by decreasing supply voltages, MOSFET threshold voltages (V_ts) have continually dropped *(Fig. 1, again)*. As the V_t's magnitude de-

COMPARISON OF TWO MINIATURE POWER-MOSFET GENERATIONS

Attribute	Little Foot	Lite Foot
Footprint	8-lead SOIC  28.8 mm^2	8-lead TSSOP  19.2 mm^2
Generation	II	IV
Power (W)	2	1
BV_{dss} (V)	20	12
Maximum V_{gs} (V)	20	8
Million cells/in.^{2}	3	6.7
I_{ds} (mΩ) (at V_{gs} of 4.5 V)	110	60
I_{ds} (mΩ) (at V_{gs} of 2.7 V)	—	100

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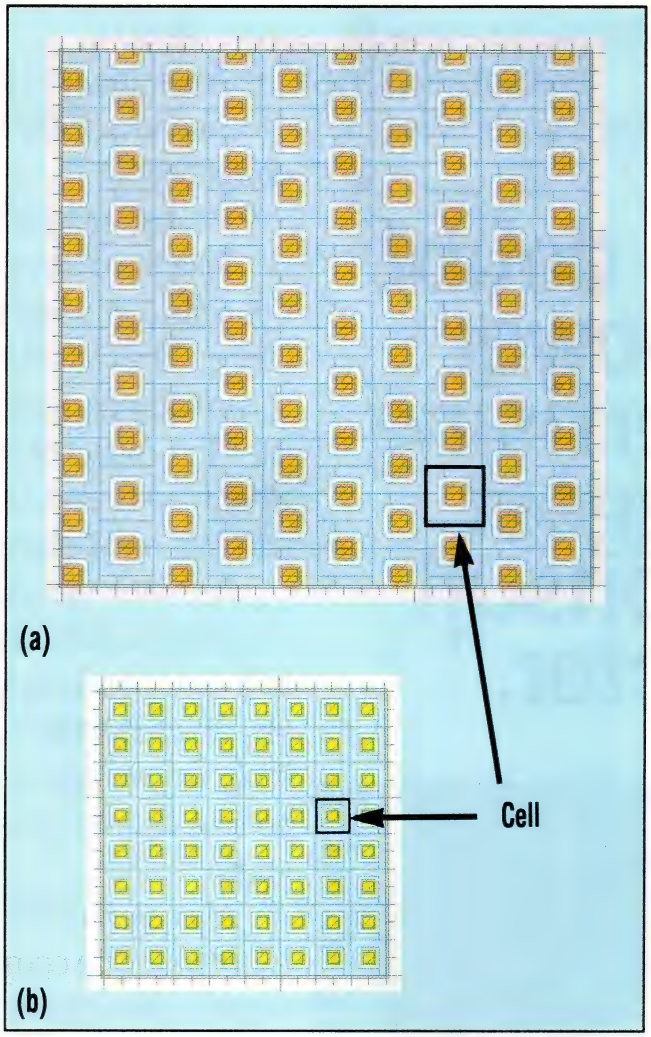
creases, its acceptable variation also must decrease. Tighter V_t tolerances are required to guarantee an on-resistance specification at a V_{gs} of –2.7 V.

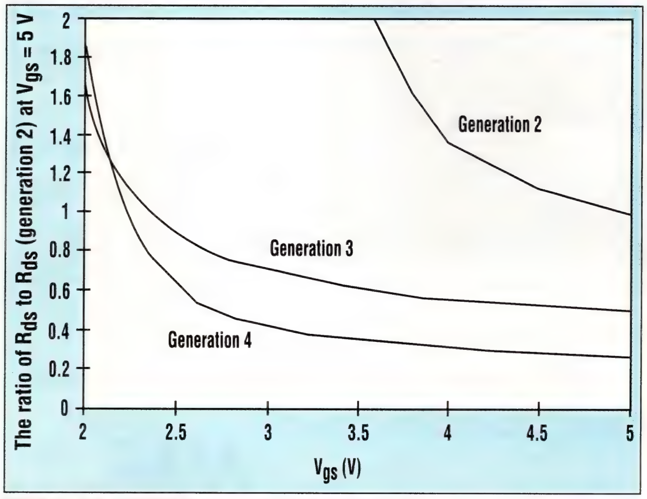
Prevention of punch-through breakdown in a submicron double-diffused channel requires that the dopant profile be controlled accurately. To ameliorate the threshold versus punch-through problem, the gate oxide of the power MOSFET also is scaled in accordance with its breakdown rating. By employing a thinner oxide, a higher channel doping can be used for the same threshold target, thereby reducing the possibility of channel leakage. However, the thinner oxide limits the maximum gate-to-source voltage, in this case to 8 V, rather than the more common 20 or more volts.

Beyond its optimization for lower gate drives, the thinner gate oxide raises the transconductance (g_m) and reduces the $R_{DS(on)}$ of the FET's channel. Because the increased channel-doping concentration suppresses the onset of punch-through, the epitaxial-layer doping can be raised to a concentration approaching theoretical avalanche breakdown. The higher doping in the epitaxial drain reduces the series drain resistance, providing a further decrease in the total $R_{DS(on)}$. Similar optimization can be performed at any given voltage rating.

Because DMOSFET on-resistance is proportional to the 2.7 power of the breakdown voltage for voltages below 60 V, a slight reduction in the voltage rating of a DMOSFET can profoundly affect its specific on-resistance. This fact is evident when comparing the typical normalized (for a given die size and voltage rating) $R_{DS(on)}$ values of second-, third-, and fourth-generation p-channel DMOSFET technology versus gate drive *(Fig. 3)*.



2. A COMPARISON of Siliconix DMOSFET cell densities shows that third-generation devices with 2.5 million cells/in.^{2} (a) have become radically smaller in fourth-generation designs that feature cell densities of 6.7 million cells/in.^{2} (b).



3. ON-RESISTANCE VERSUS gate-to-source voltage, normalized for a given die area and breakdown voltage, has dropped for each new generation of low-power DMOSFETs.

At a V_{gs} of 5 V, each generation represents a 50% reduction in specific on-resistance. In just two years, second-generation p-channel DMOS technology has achieved nearly a four-fold improvement. At a V_{gs} of 3 V and below, the second-generation technology exhibits a hyperbolically increasing $R_{DS(on)}$ while the newest generation technology rises only slightly beyond its 5-V resistance. Below 2.5 V, however, even the new p-channel technology exhibits a sharp rise in $R_{DS(on)}$.

TSSOP VERSUS DIE

Without the proper package design, the package's electrical and thermal characteristics easily eclipse the advantageous rise in DMOS cell density and drop in specific on-resistance achieved by voltage scaling. With this issue in mind, packaging engineers at Siliconix began a detailed study of the conventional TSSOP package using finite element analysis (FEA) to understand its thermal, mechanical, and electrical properties. Like its pioneering work in the first power 8-lead SOIC package (Little Foot), the goal of the Siliconix effort was to optimize the package design internally while maintaining standard external dimensions.

As with Little Foot, the new TSSOP design connects some bond wires directly between the die's bonding pad and the package pins. To improve the thermal conductance between the die and the pc board (the backside of the die is the drain of the DMOSFET), the actual drain pins are formed from the copper leadframe to which the die is bonded. This

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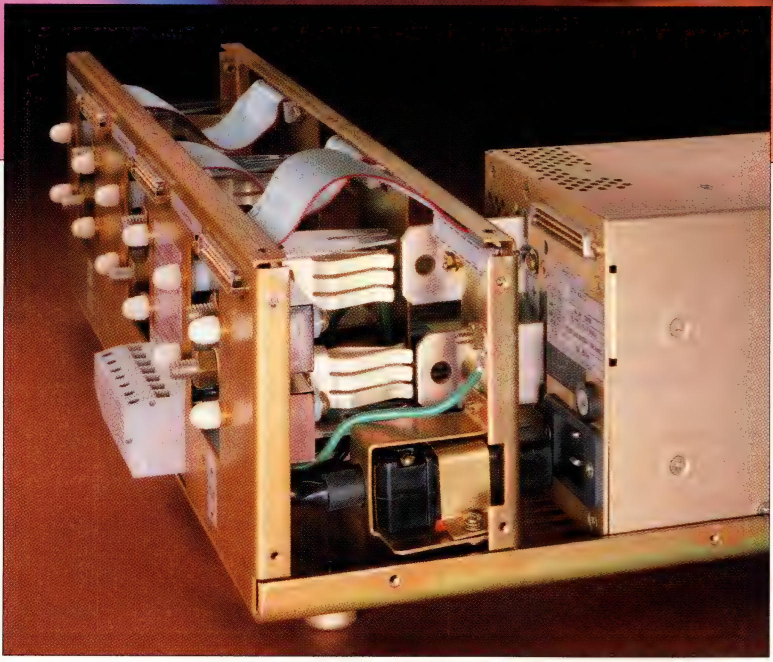

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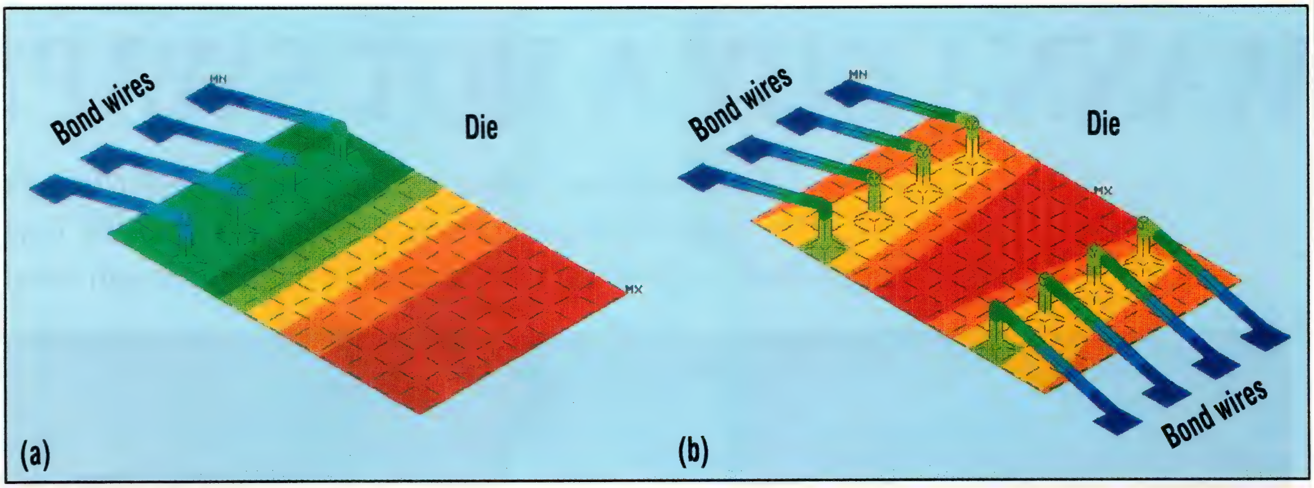

4. CURRENT DENSITY across a Lite Foot FET die was simulated with finite-element analysis, using bond wires on one side of the die (a) and on both sides (b).

technique also minimizes the contribution of package lead resistance to the effective on-resistance of the DMOSFET part.

When trying to minimize on-resistance topside, 2-mil gold leads were used between source and package pins rather than the 1.3-mil gold leads typically employed for most ICs. Moreover, most power devices use one or more 5-to-20-mil-thick aluminum bond wires. Much thought also was given to minimizing stress to prevent cracking of the plastic molding compound.

Aside from these basic considerations, special attention was paid to the distributed and spreading resistance effects in the final device. Spreading resistance is a phenomenon in which the effective resistance of a conductive material is increased due to a non-uniformity in current density throughout the material. In a vertical DMOSFET, the entire top surface of the die is the source metal. Theoretically, it connects, in parallel, each and every source/body cell of the FET. If the metal resistance is small when compared with the transistor's channel resistance, the surface of the DMOS can be considered equipotential, and multiple bond wires can connect the die to its package terminals. But, in the voltage-scaled p-channel DMOSFET, the surface-metal resistance really can't be ignored.

An FEA study revealed that a limited number of source wire bonds on one side of the die couldn't guarantee adequate uniformity in current density across the die's top metal *(Fig. 4a)*. In these FEAs, the colors of the spectrum delineate current density. This density moves "linearly" through the spectrum from blue (representing the highest density) in the bond wires to red (representing the lowest density). Unfortunately, the TSSOP's low profile make it quite difficult to run long bond wires across the top of the die.

Ultimately, providing leads for source connections on both sides of the die solved the problem by reducing the bond length while increasing the accessibility of the bonds to all parts of the die surface *(Fig. 4b)*. These figures illustrate the current uniformity in the top metal predicted by the FEA program ANSYS for the one side *(Fig. 4a, again)* and the symmetrical source-bond-wire arrangements *(Fig. 4b, again)*. Clearly, the multiple-bond-wire configuration is superior in current uniformity and therefore possesses lower effective on-resistance.

The on-resistance of Lite Foot at 2.7 V is slightly better than that of the 8-lead Little Foot at 4.5 V. This result is consistent with a 4X improvement from the second- to the fourth-generation p-channel technology when considering the 50% die-size reduction required by the smaller package *(see the table)*. The table compares the performance characteristics of a single p-channel Lite Foot to its closest predecessor, the SO-8 Little Foot. The table also includes a scaled-area comparison of the board space required by each package type, including the "keep out" area surrounding each one. "Keep out" area is the space around a surface-mounted IC that must be dedicated for use by the handling equipment.

DIG THE TRENCHES

While this discussion focuses on a 12-V, 6.7-million-cell/in.^{2} process, Lite Foot technology also is compatible with devices offering higher-voltage ratings. It will be available as both single and dual p-channel DMOSFETs, single and dual n-channel FETs, and as complementary (power CMOS) pairs. While dense planar DMOS technology offers distinct advantages in low-threshold-voltage devices, non-planar structures (i.e., trench MOSFETs) will offer even greater cell densities in higher-voltage (60-V) applications. The TSSOP package was codeveloped with both technology families in mind.

The lost surface area required by the polysilicon-gate electrode limits the performance of planar DMOSFETs. Ideally, as improvements in photolithography become available, the DMOS cell's density can be increased to achieve greater gate width (W) per unit area (A). To maximize the benefit of density improvements, both the source/body cell opening and the gate dimension must be scaled together. Ideally then, increasing the geometric packing density (W/A) should produce a commensurate decrease in on-resistance of the FET.

Unfortunately, in a planar DMOS structure, current emerging from the double-diffused surface-channel located under the gate must turn and flow vertically between two adjacent body diffusions. The pinching effect of this "neck" (or JFET region, as it's commonly called) results in an increase in the on-resistance of each DMOS cell.

While this rise in per-cell resistance is somewhat offset by a larger number of cells, further reduction in the polysilicon-gate dimension reaches an optimum point beyond which the specific on-resistance actually increases. In a planar DMOS structure, increased cell density doesn't necessarily result in a better-performing product.

One way to offset this effect is to scale the planar DMOS cell density by decreasing the target breakdown specification. For the 6.7 million cell/in.^{2} technology, a breakdown voltage below 25 V is preferred, although further optimization may be possible. And over time, technology improvements may push the low-voltage DMOS density to 8 to 11 million cells/in.^{2}—beyond which would produce little added benefit.

This density is considered the practical "scaling limit" of planar DMOS. It's based on mask layer-to-layer registration variance, doping-control limits, and the difficulty in controlling the double-diffused channel profile for extremely shallow junctions. The challenge to increased cell density is even greater at 60 V. At that level, the epitaxial layer is more lightly doped and the pinching effect is more pronounced.

NO JFETS

Another version of DMOS technology, trenched or "U-groove" power FETs, can altogether eliminate the JFET limit. In such a device, conduction is purely vertical along the side of the oxide-filled trench, thus eliminating the JFET effect. Trench use cuts this gate dimension by a factor of two to three relative to the comparable spacing in voltage-scaled planar DMOS. Accordingly, an increase in trench DMOS cell density corresponds to a commensurate decrease in resistance.

While this density increase is relatively small, performance improves substantially. By using such a structure, specific on-resistances below 1 mΩ/in.^{2} are possible, resulting in a 60-V trench MOSFET that's superior to a 20-V planar MOSFET. Theoretical density limits far exceed any competitive technology. While the trenched power MOSFET has been bandied around in academia for a number of years, only now is it becoming a manufacturable product. The development of this proprietary technology by Siliconix required over eight years of intensive R&D.

Though the trench DMOS has been used to achieve the lowest on-resistances ever reported using large power packages, its design works in synergy with the Lite Foot package, where small area is paramount. Small-area trench devices in the 8-lead TSSOP will surpass the accomplishments of their larger SO-8 planar DMOS predecessors. The Lite Foot package has been engineered to be forward-compatible with trench technology, again addressing the key issues of interconnect and package resistance associated with distributed effects in the top metal and the package.

Nonetheless, the goal of today's surface-mount power-MOSFET technology is to expand current-handling capability, not power dissipation. In fact, it's much better if power isn't dissipated at all. Ultra-low on-resistance voltage-scaled planar and trench DMOS make such a goal a reality.☐

PRICE AND AVAILABILITY

In quantities of 10,000, the Si6433DQ p-channel FET in the 8-pin TSSOP goes for $1.25 each. Sample quantities are available. Dual p-channel, single and dual n-channel, and duals with each type of FET will be available in the TSSOP within 90 days at similar prices. The first trenched (60-V) devices will be out by the end of the year.

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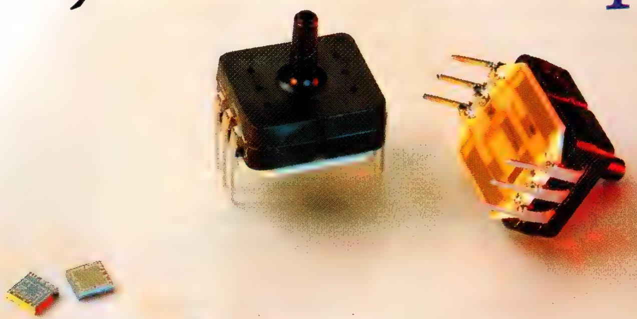

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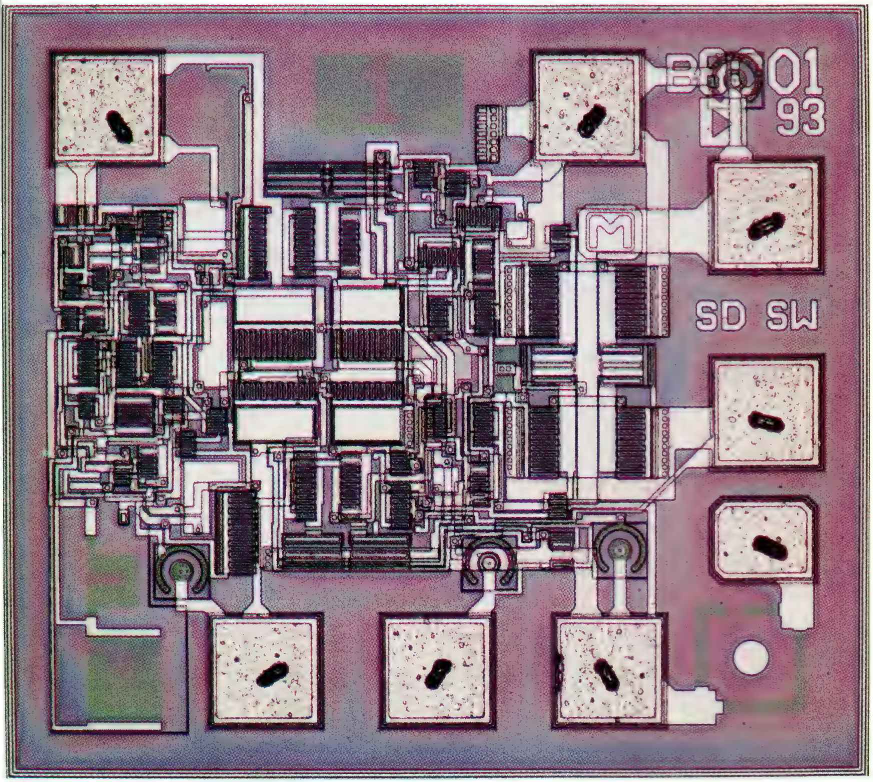

COURTESY: ANALOG DEVICES

FRANK GOODENOUGH

HIGH-PERFORMANCE COMPLEMENTARY BIPOLAR AND BIPOLAR/CMOS PROCESSES REQUIRE GREATER DESIGNER KNOWLEDGE.

SILICON, ANALOG PROCESSES ARE BECOMING MORE SOPHISTICATED

It's been said that users really don't care what's inside an IC. *So then why do analog, mixed-signal, and even digital product and system designers need knowledge of analog/mixed-signal IC processes?*

For starters, in these times of 50-MHz-and-up clocks, purely digital systems no longer exist. Even though they handle digital signals, devices such as clock drivers, clock and data-recovery ICs, and analog read-channel ICs basically employ analog-circuit techniques. Even a RAMDAC, although today largely digital, still contains a trio of state-of-the-art digital-to-analog converters at its heart. Wireless and RF ICs, just now coming of age, also join the ranks of these devices.

Judging from the performance advances being made in standard, complementary bipolar (CB), and complementary bipolar/CMOS (CBiCMOS) processes, knowledge about a process may indeed be critical. While standard bipolar processes offer 600-MHz devices, CB and CBiCMOS processes now can offer devices with f_ts of up to 10 GHz. Such processes, which provide both npn and pnp transistors, do have their pros and cons as well as various limitations *(Tables 1 and 2)*. Then there are those analog and mixed-signal bipolar and biCMOS processes with npn-only transistors offering even greater performance levels. However, these will be discussed in a future report.

TABLE 1: COMPLEMENTARY BIPOLAR (CB) ANALOG AND MIXED-SIGNAL PROCESSES

Company and process name	Type of isolation	Type of device(s)	Process* availability	Device f_t (GHz)	Device beta (β)	Device V_A (V)	βV_A product	Practical operating voltage (V)	Other process devices and features
AT&T CBIC-V2	Junction	Vertical npn Vertical pnp	2,3	10 4.3	118 45	27 11	3200 500	11	ESD diodes, thin-film resistors, MNOS and MOM capacitors, two metal levels
CBIC-U2	Junction	Vertical npn Vertical pnp	2,3	3.5 2.7	125 35	40 14	5000 500	11	Same as CBIC-V2
Analog Devices CB	Junction	Vertical npn Vertical pnp	4	0.65 0.6	175 175	57 57	10,000 10,000	30	n-channel JFETs, buried Zener diodes, thin-film resistors, MOM capacitors, two metal levels
XFCB	SOI, bonded wafers, trenches to oxide	Vertical npn Vertical pnp	4	4.5 3	110 55	80 25	8800 1400	12	Same as CB plus Schottky diodes
Elantec (No process name)	SOI, oxide tubs (DI)	Vertical npn Vertical pnp	4	0.6 0.6	NA	NA	NA	30	—
(No process name)	SOI, oxide tubs (DI)	Vertical npn Vertical pnp	4	4 3	NA	NA	NA	24	—
Harris Semiconductor EBHF	SOI, oxide, tubs (DI)	Vertical npn Vertical pnp	3,4	0.6 0.3	250 150	NA NA	NA NA	24	JFETs, MOS capacitors, buried Zener diodes, thin-film resistors, two metal levels
VHF	SOI, oxide, tubs (DI)	Vertical npn Vertical pnp	3,4	1.3 1	100 80	80 20	8000 1600	15	Same as EBHF
UHF	SOI, bonded wafers, trenches to oxide	Vertical npn Vertical pnp	3,4	8 5	100 100	40 20	4000 2000	10	Same as EBHF
Linear Technology CB	Junction	Vertical npn Vertical pnp	4	0.6 0.6	100 100	300 100	30,000 10,000	30	JFETs, MOS capacitors, thin-film resistors
National Semiconductor VIP I	Junction	Vertical npn Vertical pnp	4	0.35 0.175	150 80	200 60	30,000 4800	30	—
VIP II	Junction	Vertical npn Vertical pnp	4	0.7 0.35	150 80	200 60	30,000 4800	30	—
VIP III	Junction	Vertical npn Vertical pnp	4	3 1.5	NA	NA	NA	30	—
Synergy Asset	Junction with oxide trenches to substrate	Vertical npn Vertical pnp	3,4 1	17 7	200 100	40 20	8000 2000	10	JFETs, MOS capacitors
Texas Instruments Excalibur II	Junction	Vertical npn Vertical pnp	4	0.4 0.1	NA NA	NA NA	30,000 15,000	40	JFETs, MOS capacitors, thin-film resistors, two metal levels
Excalibur III	Junction	Vertical npn Vertical pnp	1	1.8 0.5	NA NA	NA NA	20,000 6000	60	Same as Excalibur II
Tektronix/Maxim Integrated Products C-PI	Junction	Vertical npn Vertical pnp	2,3,4	12 8.5	120 29	18 12	2160 348	5	JFETs, thin-film resistors, Schottky diodes, dense logic
United Technologies Acute	SOI, bonded wafers, trenches to oxide	Vertical npn Vertical pnp	2	3 2	200 150	500 85	100,000 12,750	30	Thin-film resistors, two metal levels

* Process availability: 1 = under development; 2 = foundry; 3 = semicustom ICs; 4 = merchant-market ICs.

DI = dielectric isolation; ESD = electrostatic discharge; MNOS = metal-nitride-oxide silicon; MOM = metal-oxide-metal; SOI = silicon-on-insulator; NA = not available.

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The silicon processes described in the tables may dominate higher-performance analog and mixed-signal applications, but they do compete with other processes in certain "niche" performance sectors. One of these is gallium arsenide, which is used in ICs with the highest speed and widest bandwidth. And, soon, silicon germanium is expected to fan the competitive flames even more.

If system designers combine some capabilities of various IC processes with the specifications of the ICs these processes spawn, they'll have a better understanding and a more intuitive "feel" for the limits and the true capabilities of these ICs. If they're planning an ASIC or some other form of semicustom or custom chip, many reasons dictate why they must "know" the process.

For instance, the better they understand the capabilities and cost of the available processes, the better they can decide which process to choose for maximum performance and minimum cost. In addition, a greater understanding of a process allows designers to work better with the process supplier to optimize an IC's performance and minimize its cost. That is, a designer can trade off performance against cost. Moreover, this kind of knowledge helps designers partition a chip set *(see*

TABLE 2: COMPLEMENTARY BIPOLAR CMOS (CBiCMOS) ANALOG AND MIXED-SIGNAL PROCESSES

Company and process name	Type of isolation	Type of device(s)	Process* availability	Device f_t (GHz)	Device beta (β)	Device V_A (V)	βV_A product	Practical Operating voltage (V)	Other process devices and features
Analog Devices CBCMOS1E	Junction	Vertical npn Vertical pnp MOS	4	0.6 0.3	250 130	100 60	25,000 7800	30	Buried Zener diodes, MOS capacitors, thin-film resistors, buried layer. Effective CMOS gate length is 2.2 μm
CBCMOS2E	Junction	Vertical npn Vertical pnp MOS	4	2.5 0.8	NA	NA	NA	NA	Same as CBCMOS1E except for 2-μm effective CMOS gate length
Exar CBiCMOS	Junction	Vertical npn Vertical pnp MOS	3,4	5 1.5	100 100	50 25	5000 2500	12	Effective CMOS gate length is 1.2 μm
Harris Semiconductor HBC-10	Junction	Vertical npn Vertical pnp MOS	3,4	5 1	120 40	50 NA	6000 NA	10	Buried Zener diodes, MOS capacitors, thin-film resistors. Effective CMOS gate length is 1.4 μm
Hughes Microelectronics CBiCMOS	Junction with oxide trenches to epitaxial layer	Vertical npn Vertical pnp MOS	2,3	4.5 2.4	405 90	20 40	8300 3600	10	JFETs, Schottky diodes. Effective CMOS gate length is 2 μm
Motorola Semiconductor CBiCMOS	Junction	Vertical npn Vertical pnp MOS	NA	8 2	125 25	80 45	10,000 1125	5	JFETs, Schottky diodes. Effective CMOS gate length is 0.8 μm
National Semicondutor ABIC	Junction	Vertical npn Vertical pnp MOS	4	12 5	90 NA	40 NA	3600	5	Effective CMOS gate length is 0.8 μm
CS80	Junction	Vertical npn Vertical pnp MOS	4 1 4	7 4	NA NA	NA NA	NA NA	5	Same as above
Raytheon Semiconductor CBiCMOS/ CBiCMOS(SD)	Junction	Vertical npn Vertical pnp MOS	3,4/1	4/8 1.5/4	60/100 30/75	60/80 15/30	3600/8000 450/2250	12	Schottky diodes, MOS capacitors, thin-film resistors, two metal layers. Effective CMOS gate length is 1.6 μm
Texas Instruments LinBiCMOS	Junction	Vertical npn Vertical pnp MOS	4 1	1 NA	80	160	12,800	5	MOS capacitors. Effective CMOS gate length is 2 μm
VTC CBP1	Junction	Vertical npn Vertical pnp MOS	5	11 2.5	150 65	30 11	4500 715	5	Thin-film resistors, oxide capacitors, Schottky diodes. Effective CMOS gate length is 1 μm

* Process availability: 1 = under development; 2 = foundry; 3 = semicustom ICs; 4 = merchant-market ICs; 5 = in-house use.

NA = not available

"For analog designers, process knowledge can be crucial," p. 102).

A CLOSER LOOK

Standard-analog bipolar processes produce devices that are relatively slow by today's standards. These bipolar junction-isolated processes are comparatively simple, requiring only a few mask steps. On it, vertical npn transistors can be designed with a unity-current-gain frequency (f_t) between 200 and 600 MHz. Lateral pnp transistors at least an order of magnitude slower also are available. In fact, most offer JFETs as options, and others provide Schottky diodes. Virtually all provide diffused resistors, and some also can be used to build implanted or polysilicon resistors. In addition, a few offer MOS capacitors and/or thin-film resistors.

A CB process, on the other hand, is more complex. Its high-speed/wideband technology allows it to build fast vertical pnp transistors as well as fast vertical npn transistors. Modern CB processes produce devices with f_ts that run from 600 MHz to over 10 GHz. A few processes employ some type of silicon-on-insulator (SOI) for isolation, while most use a form of junction isolation that may include oxide-filled trenches. Many offer all of the extra features of standard bipolar processes *(Table 1, again).*

Most CB processes were developed from basic process technology. However, the majority of CBiCMOS processes are either CB technologies that incorporate CMOS, npn-equipped biCMOS processes that add a vertical pnp transistor, or a CMOS process to which both npn and pnp transistors were added. In available CBiCMOS processes, transistor f_ts run from 1 GHz to over 10 GHz. In most cases, these processes are "modular." That is, IC designers need only use the devices required by their circuits. Limiting the types of devices available on a process can simplify that process, raising yields and lowering die cost *(Table 2, again).*

When comparing high-performance analog and mixed-signal semiconductor processes, several device/process specifications or figures of merit determine speed and precision. In a MOS process, effective gate length (L_{eff}) determines speed and bandwidth, while the ratio of gate length to width determines analog performance. Although an f_t of a MOS device is usually available, it's generally a function of L_{eff}.

For maximum speed and/or analog precision, designers must turn to bipolar transistors. Here, device f_t determines speed/bandwidth, while the product of its current-gain beta (β) and its Early Voltage (V_A) determines analog precision. Even though f_t remains the most common indicator of a transistor's bandwidth, two devices from a different (or even the same) process may have the same f_t. However, one may provide superior bandwidth in an IC. This is because the truly faster device possesses lower parasitic capacitances from junction to emitter, junction to substrate, and junction to collector; respectively known as C_{je}, C_{js}, and C_{jc}.

A high-current-gain β is, of course, desirable for all bipolar transistors, but it's mandatory when precision analog tasks are at hand. However, the product of β and Early Voltage, βV_A, is even more important. The higher the V_A, the better the current sources that lie at the heart of most analog ICs.

Early voltage is a figure of merit. It indicates how parallel a bipolar-transistor's family of V-I curves are to the horizontal (collector-emitter voltage) axis of the graph on which they're plotted. If the nearly horizontal portions of the curves are extended to the left of the vertical (collector-current) axis, they will all meet on the X-axis at some voltage, which is the Early Voltage. If the curves were exactly parallel to the collector-emitter voltage axis, they would not meet if extended, indicating a V_A (and thus a βV_A) of infinity. This would imply the ability to build perfect current sources.

KNOW βV_A

For even reasonable analog performance, βV_A should be at least 500; for true precision, it should exceed several thousand. V_A tends to track rated collector-emitter breakdown voltage. The original, slow, standard bipolar processes, some with f_ts below 200 but rated at 40 or more volts, often had f_ts of over 20,000. On the other hand, many of today's fine-geometry, high-speed, but low-voltage processes provide bipolar transistors (particularly pnp transistors) with βV_A products as low as 500. These devices truly challenge the high-performance analog-IC designer.

The V_A of these low-voltage devices throw IC designers another curve—nonlinearity. That is, the high-voltage (right-hand) end of each V-I curve usually increases in slope as the breakdown voltage is approached, representing a significantly lower V_A. One of many effects is an additional source of op-amp distortion when approaching maximum output swing. In many applications, particularly when operating from low supply voltage, an IC designer usually strives for every extra millivolt of low-distortion swing from these low-voltage transistors.

Complementary-bipolar processes represent the ultimate high-speed/precision processes for analog ICs. Adding CMOS brings them into the mixed-signal world. Moreover, with CMOS, sampling data converters, multiplexers, and integrators can be built. JFETs often perform similar tasks in a CB process.

Today, complementary-bipolar technologies that are junction-isolated also rule the roost as far as f_t is concerned. AT&T's CBIC-V2 process provides npn- and pnp-transistor f_ts of 10 and 4.3 GHz, respectively. Tektronix's recently-announced C-PI process sports npn- and pnp-transistor f_ts of 9 and 5.5 GHz, respectively. Both are available on a foundry and semicustom basis. AT&T's processes have been around the longest, though, with merchant-market op amps being developed by such semiconductor suppliers as Analog Devices, Burr-Brown, Comlinear, Harris, and others.

It will be interesting to see what devices appear from the Tektronix process, particularly if the sale of Tektronix's fabrication facility to Maxim Integrated Products is consummated. For several years, Maxim has been building op amps and comparators on VTC's 12-V CB process (not listed in the tables), which offers 6-GHz npn and 1-GHz pnp devices. In addition, Synergy is adding a 7-GHz vertical pnp device to its 17-GHz npn-only process. The βV_A of the pnp transistor is expected to run about 2000. In contrast, the CBIC-V2 pnp device comes in at only 500, and the C-PI process has a mere 350. Both Synergy's ASSET process and Tektronix's C-PI process provide dense and fast bipolar logic, such as ECL and current-mode logic (CML).

BONDED WAFERS

So far, only two major analog/mixed-signal IC suppliers, Analog Devices and Harris Semiconductor, have moved to SOI processes to obtain speed and bandwidth. Harris Semiconductor made the transition to SOI years ago (at the time it was known as Radiation Inc.), developing polysilicon-handle dielectric isolation (DI) to provide radiation-hardened ICs.

Each transistor in a DI process is isolated electrically from all other transistors in an oxide tub. Not only are these ICs radiation-hardened, but they're also free from dc parasitic junctions, making possible simple CB processes. In addition, ac parasitic capacitances of the transistors are significantly reduced, boosting speed and bandwidth.

For over a decade, Harris Semiconductor dominated the high-speed op-amp arena thanks to the elimination of parasitics. That dominance went unchallenged until about six years ago, when a number of other junction-isolated processes began to emerge.

Less than two years ago, Harris Semiconductor moved to the newer bonded-wafer process, and Analog Devices went that route last fall. In a bonded-wafer SOI process, designers can build transistors in silicon lying on an oxide substrate. The devices are isolated from each other by oxide-coated trenches, back-filled with polysilicon, which are etched between the die's surface and the substrate.

FOR ANALOG DESIGNERS, PROCESS KNOWLEDGE CAN BE CRUCIAL

It used to be common to have analog designers working side by side with process engineers. Such a situation provided the perfect marriage of process understanding and design methodology, allowing designers to tweak the application of a chip in a system for optimum performance.

Times have changed. Today, while chips are produced at an amazingly fast pace, and the desire to build bigger and better systems than the competition continues to be a part of the picture, it's almost impossible to have this type of relationship between a designer and a process engineer.

What does this mean to the typical analog design engineer? According to some, it translates into a new breed of engineers who are equipped with the knowledge of semiconductor processes, and then know how to use it to make their systems better. As Lee Stoian, director of data-acquisition design, National Semiconductor, puts it, "Today's analog designers need to have an understanding of the processes to get the most out of the chips they're designing with." For the many designers who push the performance limits of a chip, it's essential that they know the physical characteristics that define the chip, as well as understand what these characteristics mean and how they affect the chip's operation.

Some of the benefits of this knowledge are obvious. For example, with process understanding comes the ability to extrapolate the performance of parts that haven't yet been released. It also provides insight into the capabilities or limitations of a part not necessarily cited on a data sheet. In addition, designers can avoid the inevitable pitfalls that arise all too often from ambiguous specifications.

According to Scott Kreps, director of technology development at Harris Semiconductor, "This knowledge helps designers foresee and avoid potential problems which may have gone unnoticed while modeling the system." Inevitably, any design will degrade by the time it goes from layout to fabrication. Such problems as mismatch and failure to account for breakdown voltage during layout are just two problems an unaware designer could face. Basically, "if you have knowledge of the processes than you have insight into what's not on the data sheet," says Kreps.

One situation, related by the Harris Semiconductor Group, Melbourne, Fla., arose a few years ago when they joined forces with GE Solid State, Somerville, N.J. At the time, each organization used two completely different processes to make the same part. Each process had its own idiosyncrasies that affected the operation of the part in different ways. Problems began when customers, who had previously used one particular part, ended up with the other one. Because the part was made with a different process, it caused problems that had never existed before when integrated into the company's various systems.

Kerry Lacanette, manager of data-acquisition applications engineering at National Semiconductor, relates a much different story. Using their knowledge of semiconductor processes, National's designers were able to take a traditional analog-to-digital converter and develop a successive-approximation converter with self-calibrating techniques. In effect, having the knowledge enables designers to "not get stuck with building blocks. And, it allows designers who design an analog device the foresight to be able to add digital components down line."

In all fairness, there's another side to the story. Not everyone agrees that designers need to have some knowledge of semiconductor processes to survive in the analog world. In actuality, as

The effect of parasitic capacitance is well illustrated by comparing AT&T's CBIC-V2 process, Harris Semiconductors' UHF-1 bonded-wafer process, and Analog Devices' bonded-wafer XFCB process *(Table 1, again)*. The first two processes provide transistors with significantly higher f_ts, but the speed and bandwidth of available op amps from each process is similar due to the lower junction-to-substrate capacitance of Analog Devices' XFCB process. In addition, according to Analog Devices, the die size on their XFCB process is smaller than the other two processes.

The 17-GHz Synergy ASSET process walks a path between SOI and junction isolation. Unlike bonded-wafer SOI processes, the ASSET process employs oxide-filled trenches from the die surface to the silicon substrate, rather than into an insulating-oxide substrate. Ac parasitics (capacitance) are reduced, but dc parasitics remain. Notwithstanding, when the process is available with the 7-GHz pnp transistor, it will be the fastest analog CB process.

The degree of match between the f_t of the pnp and the npn transistors in these processes also affects the performance of their ICs. If their f_ts aren't well matched, high-frequency distortion can occur in complementary circuits. In many of the older and slower processes, npn- and pnp-transistor f_ts are identical. Most of these processes are "high-voltage" processes designed to handle typical ±15-V analog power-supply rails. But the fastest processes can only handle 5 to 10 V between such rails.

HIGH VOLTAGE

Nevertheless, three new complementary high-voltage processes offering additional bandwidth at 30 V have come onto the scene recently. Each has taken a different tack. National Semiconductor's VIP III process employs junction isolation to achieve npn- and pnp-transistor f_ts of 3 and 1.5 GHz, respectively. However, while βV_A products aren't available for devices made on the VIP III process, National Semiconductor built a high-speed micropower op amp on this process that also handles high voltages.

United Technologies' ACUTE process is the first high-voltage complementary-bipolar process to use bonded-wafer SOI techniques. It provides nicely matched npn- and pnp-transistor f_ts of 3 and 2 GHz, respectively, along with superior βV_A products of 100,000 and 12,750, respectively. The third process, Texas Instruments' Excalibur III, not only increases transistor f_ts over earlier versions of the Excalibur process, but also raises the voltage rating from 40 V up to 60 V.

A fourth new process, developed by Hughes Microelectronics, actually is a CBiCMOS process. It takes the approach that Synergy employs, using an oxide-filled trench between the surface of the die and an epitaxial layer grown on the silicon substrate *(Table 2, again)*. This 10-V process not only offers npn- and pnp-transistor f_ts of 4.5 and 2.4, respectively, but also respective βV_As of 8300 and 3600. This kind of device performance simplifies the task of analog-IC designers.

The majority of CBiCMOS processes sport interesting features, further underscoring the fact that they represent the ultimate mixed-signal IC process. However, it should be noted that many of these processes are high-speed biCMOS processes with a vertical pnp transistor in development. As noted earlier, virtually all are modular processes.

Both Analog Devices' CBCMOS1E process (developed at its PMI Div.) and the Exar CBiCMOS process have been around for quite some time. The CBCMOS1E process is used as a general-purpose analog process that takes advantage of its modularity. The same is true of Raytheon's CBiCMOS and its next-generation CBiCMOS (SD) processes. In fact, Raytheon added CMOS to a CB process that's used in a number of products. The advanced SD version of CBiCMOS ups both the f_t of the transistors and their βV_A product. On the other hand, Harris Semiconductor's HBC-10 process was originally designed as a CMOS process to which the company added CB capability.

The development of National Semiconductor's biCMOS/CBiCMOS process has taken dual paths. The company's ABIC process added CMOS to a bipolar technology, and its CS80 process incorporated bipolar devices into a CMOS process. The former aims at RF applications while the latter targets mixed-signal applications. Though both processes are now at 0.8-μm line widths, they will follow the reduced-gate-length technologies provided by digital CMOS.☐

pointed out by Al Haun, a spokesman for Analog Devices, unless you're pushing the edge of technology or using a part at its performance limit, this knowledge wouldn't even be needed.

Tim Johnson, manager of mixed-signal ASIC design at Harris Semiconductor, sums it up best. "It's really a 70/30 split. Seventy percent of the designers in the analog world deal with everyday designs, while thirty percent work on the cutting edge of new technology. Only the thirty percent are the ones who really need to understand the semiconductor processes." It's like the "don't ask/don't tell" rule of the analog world. Seventy percent of the designers either don't ask or don't want to know any process information, and most manufacturers don't necessarily volunteer this information unless asked.

As analog technology continues to grow at a feverish pace, and as designers demand the maximum performance out of chips they design into their systems, it will become increasingly important to understand semiconductor processes. If nothing else, the added knowledge will help avoid potential pitfalls in designs, and allow for the development of clever systems to address some of today's most difficult problems.

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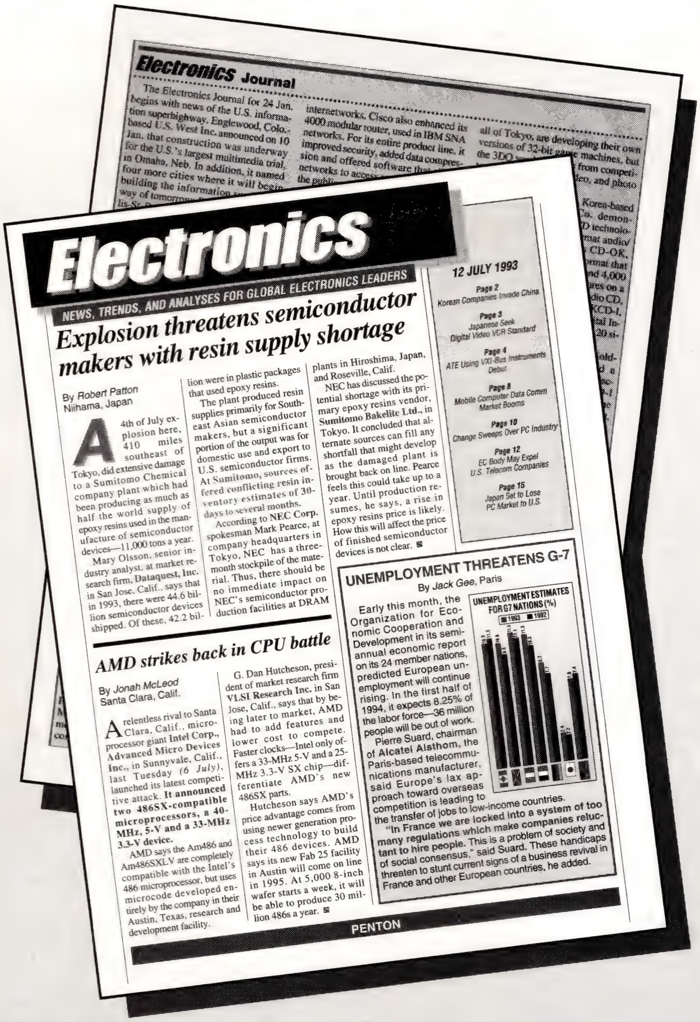

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Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear. ■

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp.**, **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year. ■

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of **Alcatel Alsthom**, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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SIMULATE LASER-TRIMMED RESISTORS WITH SPICE

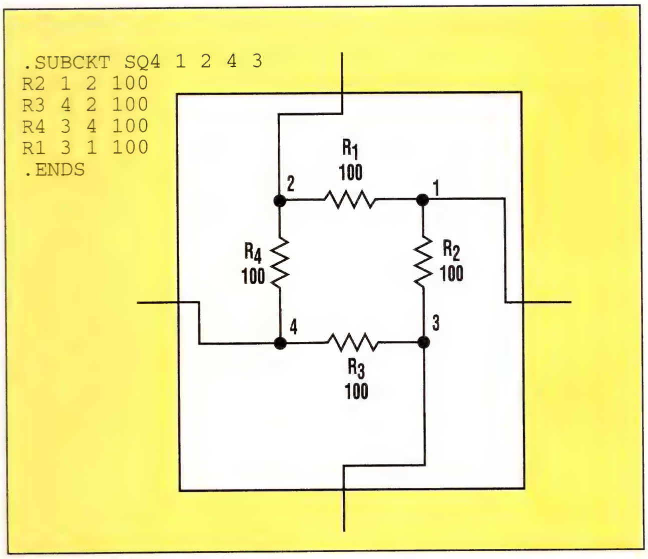
To simulate physical systems using Spice, engineers create electrical analogs of the physical parameters. The thermal analysis of a packaged MOSFET, for example, entails calculating the thermal capacitance and thermal resistance of various materials in the package. Adding ideal current and voltage sources to the analysis completes the circuit. Although the resulting schematic effectively simulates the physical system, it's merely a symbolic diagram. It doesn't enhance the physical view of the system's operation.

This article shows how a design engineer can use Spice to simulate thick- or thin-film resistors that have laser trims or complex shapes. The method employs a subcircuit technique to address this issue. Using any one of a number of Spice simulation software packages (which feature schematic capture, the ability to create subcircuits and symbols, and to copy these symbols into groups), a circuit schematic can be developed by the design engineer that also serves as a representative picture of the resistor as it would appear printed on a substrate.

The subcircuit technique is useful as a tool to help solve real-world problems in designing resistors. Moreover, with this technique, a designer using Spice can easily determine resistor values with variations in geometry or laser-trimmed values.

Recall that a square of resistor material is merely a chunk of the material with equal dimensions on each side and some specified thickness. If the resistance of the material is 100 Ω/square at the specified thickness, it really makes no difference whether each side measures 0.1 cm or 10 cm. The total resistance of the chunk still turns out to be 100 Ω.

Using the relations:
Squares = L/W, and
Ω = Squares × (Ω/Squares),
where L = length and W = width,



```
.SUBCKT SQ4 1 2 4 3
R2 1 2 100
R3 4 2 100
R4 3 4 100
R1 3 1 100
.ENDS
```

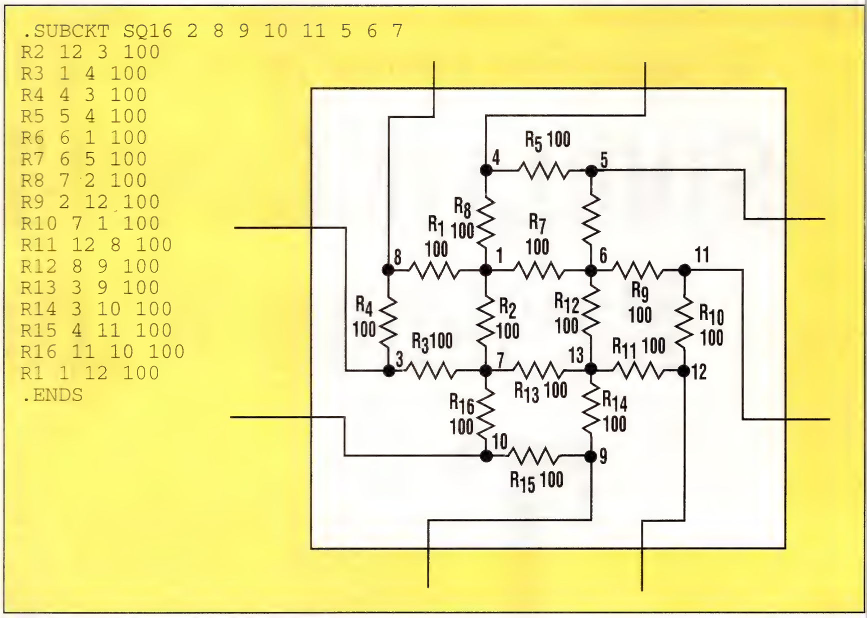
1. THIS SYMBOLIC representation of one square of resistor material is based on a schematic of a four-resistor square. A quick inspection shows that the equivalent resistance across opposite sides of the symbol is 100 Ω.

DENNIS EDDLEMON
Apex Microtechnology Corp., 5980 North Shannon Rd., Tucson, AZ 85741; (602) 690-8600.

the equivalent squares and resistance of a rectangular resistor may be calculated.

Unfortunately, the calculations for non-rectangular resistors aren't quite as simple. One common example is the top-hat geometry. Reference texts often refer to graphs with various curves for geometry ratios to specify the equivalent square count of the top hat. Other graphs show resistance variations as the laser-trim depth increases. But published graphs don't indicate how the value varies with laser-trimmed double-cuts, or "L"-cuts.

They also don't show effects with odd-shaped resistors. This is where building the resistor geometry in Spice shines. With the subcircuit technique, Spice not only determines rectangular and non-rectangular resistor values in a matter of a few seconds, but also displays the physical results as well.

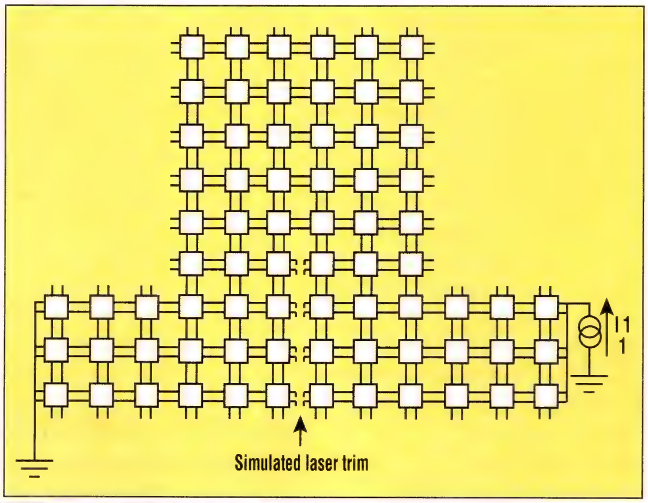


```
.SUBCKT SQ16 2 8 9 10 11 5 6 7
R2 12 3 100
R3 1 4 100
R4 4 3 100
R5 5 4 100
R6 6 1 100
R7 6 5 100
R8 7 2 100
R9 2 12 100
R10 7 1 100
R11 12 8 100
R12 8 9 100
R13 3 9 100
R14 3 10 100
R15 4 11 100
R16 11 10 100
R1 1 12 100
.ENDS
```

2. ANOTHER SQUARE of resistor material is modeled with 16 resistors to achieve greater accuracy when simulating laser cuts on complex resistor geometries. Each terminal pair must be treated as one (either connected or not connected to another symbol).

A BUILDING BLOCK

As a basic Spice building block, consider a symbol created to represent one square of resistor material *(Fig. 1).* Though the schematic of the 4-resistor "square" is shown inside the symbol, this needn't be done in practice. The schematic only serves to show the connections between the subcircuit and the symbol. By inspecting across opposite sides of the symbol, it's easily seen that the equivalent resistance of the square is 100 Ω.



3. A TYPICAL top-hat resistor is quickly and easily constructed using the copy and join steps in the subcircuit technique. While some of the terminals appear to be open-circuited, the schematic shows that they are not, Spice won't converge with open-circuited components.

A similar symbol and schematic uses 16 resistors to represent the square of resistive material *(Fig. 2).* As might be expected, the more resistors used to simulate the square, the more accurate the results will be when simulating laser cuts or complex resistor shapes. The resistor matrix must be connected at the corners to properly simulate a square of material. After all, a real square of material could be considered as an infinite number of resistors arranged in an extended but similar fashion. The symbol also serves to convert the diagonal nature of the schematic to a rectangular format, which is much more convenient for building a resistor from many squares.

Although each side of the subcircuit has multiple terminals, they must be treated as one for the subcircuit to work correctly. In other words, if one terminal is opened or interconnects to a terminal of another symbol, then the others must do the same.

Once the symbol is created, it's retrieved from the Spice software library and a short wire segment is added to each terminal. This ensures that Spice will assign a node number to the terminal. It also allows connections between square symbols to be severed to simulate trims.

Next, the symbol with its attached wire segments is copied and joined to the original. The copying and joining of symbols should continue until the complete resistor geometry is constructed.

This method was used to construct a typical top-hat resistor shape *(Fig. 3).* One end of the resistor is fed with a current source scaled for 1 A; the other end is grounded. All of the terminals at each end of the resistor must be tied together. Even though some terminals extending from some of the symbols appear to be open-circuited, the schematic of the symbol in Figure 2 shows they're not (Spice, of course, would not converge with open-circuited components).

The current source is scaled at 1 A so that the voltage read at its terminal will be the same as the total circuit resistance when each subcircuit symbol contains 100-Ω resistors. Other Ω/

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square values could be handled by scaling the current-source for different values. If, for example, the resistor material was 3 kΩ/square, the current-source would be scaled for 30 A. Scaling the current-source is preferred to altering the subcircuit resistor values each time the resistor material changes. The 100-Ω/square subcircuit described previously is chosen only for convenience. Any value would do as well with the proper scaling applied to the current source. For instance, the subcircuit resistors could be scaled for 1 Ω. Then, the voltage read at the current-source terminal would be considered to be the equivalent square count.

TESTING CORNERS

To determine the accuracy of the Spice simulation using this technique, a corner test circuit was designed to act as a calibrator *(Fig. 4)*. The test circuit has three squares, and each square is made up of 16 subcircuits. Each subcircuit contains 16 resistors. Although three squares are shown, the equivalent square count isn't three. The corner doesn't equal one square due to the current distribution in the material going around the bend. However, the circuit was constructed in this way because a corner can't exist in isolation. Also, the equivalent square count of the corner will vary slightly with the amount of material on each side of it. Yet, the value remains essentially constant when there's one or more squares at each end.

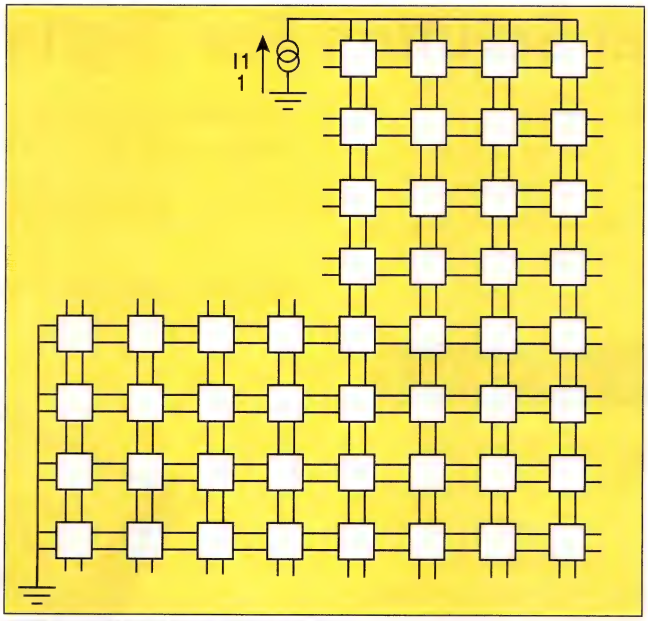
Corner test circuits were constructed and tested having total resistor counts of 64, 256, and 1024 per square. Spice reported the equivalent square counts as 0.591, 0.571, and 0.563, respectively. The actual equivalent square value for a corner is 0.559. These results give a feel for the accuracy values versus the resistor count. Several reference texts have reported the equivalent square value of a corner to be 0.65, but that's incorrect as is indicated by the Spice simulation. To relate the simulated resistor to the actual printed resistor, each symbol is assigned a physical dimension. The top-hat resistor of Figure 3, for example, was constructed with 12 symbols along the base. If each symbol (square) were assigned a dimension of 5 mils, then the base would be 60 mils long. The total height would be 45 mils and the resolution 5 mils. The resolution could then be increased by adding more symbols to increase the total symbol quantity.

For example, the total height of the top-hat could be boosted to 18 symbols (the other dimensions increased accordingly) and the resolution would increase to 2.5 mils (assuming the total height was still considered to be 45 mils).

The issue of resolution becomes important when investigating the laser-trimmed behavior of a resistor. Consider the top-hat resistor with a laser trim, where the connection between adjacent squares is opened by merely directing the short wire segments on the terminals down, instead of across *(Fig. 3, again)*. In the example, the total height of the top hat was 45 mils, with the resolution being 5 mils. This is equivalent to a laser trimming out 5 mils of the resistor with each bite. Assuming that all design requirements of the resistor are known, this analysis would be sufficient to properly design the resistor's geometry. Sometimes, though, the total requirements of the resistor design are best evaluated when compared with the operation of other circuit components that aren't precisely defined.

Many thick-film hybrid circuits need to be actively trimmed for various parameters. A case in point would be power operational amplifiers. Typical parameters that require laser trimming are offset voltage, offset-voltage drift, output-stage bias current and the thermal-shutdown temperature trip point.

Using the technique described, the resistor models to be trimmed can be inserted into the Spice schematic of the circuit. A simplified circuit schematic of the Apex PA05 illustrates this point *(Fig. 5)*.



4. A CORNER CIRCUIT, used for calibration purposes, could represent some circuit interconnecting metal path or a section of a "snake" resistor. Although the circuit appears to be made up of three identical squares, the square in the corner actually has an equivalent square value of 0.559.

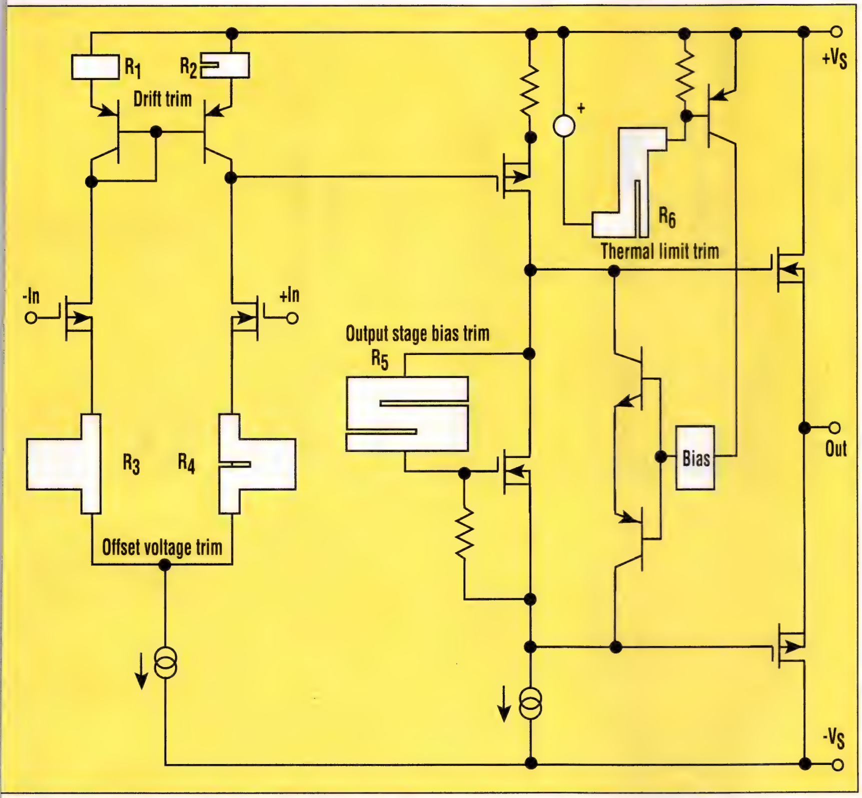
TRIM STABILITY

Laser-trimmed resistor stability is related to, among other things, the distance from the end of the laser cut to the edge of the resistor. Micro-cracks left in the resistive material at the end of the cut are prone to change the resistor value during temperature cycling and burn-in. This shift can be quite significant if the micro-crack length is large compared to the remaining uncut width of the resistor.

For trimming accuracy, the rate of change of parameter variation with laser cut bite size also must be considered. It's possible, for example, to achieve a total change in the trimmed resistor that's the required size. But, the rate of change of the trimmed parameter may be so great that with each laser bite, the parameter simply changes too fast to achieve the required accuracy. In other words, gross overtrim could result from having trimmed one bite too many.

Whenever the drift-resistors, R_1 or R_2, are trimmed, the output offset voltage also is affected. Thus, the

SIMULATING LASER-TRIMMED RESISTORS



5. A SIMPLIFIED SCHEMATIC of the Apex PA05 illustrates how the models of laser-trimmed resistors can be inserted into the Spice circuit schematic.

offset voltage must be trimmed back to zero. This interaction causes R_3 or R_4 to be trimmed more than would be otherwise expected. However, by inserting the trimmed-resistor models into the circuit, it's possible to see how much of the trim resistors remains once the circuit is trimmed to maximum.

Output-stage bias current is adjusted by trimming R_5. In this particular circuit, R_5 needs to have a wide range of possible values. In fact, the trim range is 4 to 1. This wide range is due to the variations in resistor tolerances and MOSFET threshold values. Consequently, the trim resistor was designed so that a maximum of two laser cuts would cover the range and still produce a stable resistor with acceptable trim resolution.

FIXING A PROBLEM

Resistor R_6, with its odd shape, was designed to solve a particular problem. The resistor's original design was unacceptable due to trim sensitivity and range. However, the problem wasn't discovered until after work had begun on the second substrate production lot.

This particular shape was developed by employing the methods described in this article, and it solved these problems using the available space on the substrate. The newly designed resistor was inserted into an iteration of its resistor layer, thus saving the cost of scrapping the substrate run and designing new metal masks.

Although purely mathematical means could be used to solve the particular problems of thick-film resistor shapes, trim ranges, and trim sensitivities, the method described here offers accurate solutions to what's essentially a geometrical problem. Furthermore, the visual aid is helpful in both designing and evaluating the performance of the resistor design.☐

Dennis Eddelmon, design engineer for Apex Microtechnology, holds a BA in sociology from Valparaiso University, Indiana.

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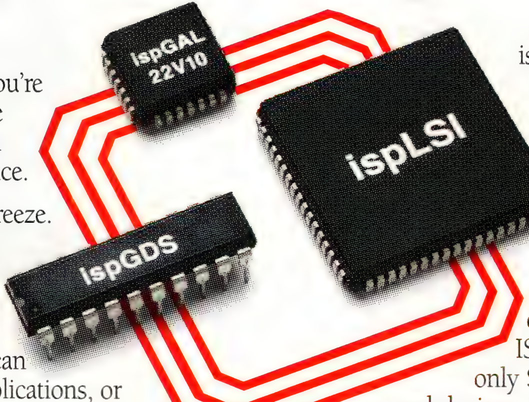

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521 ISOLATED PARALLEL ADC

MARTIN O'HARA
Newport Components Ltd., 4 Tanners Dr., Blakelands North, Milton Keynes,
MK14 5NA, England; phone: (0908) 615232, fax: (0908) 617545.

Although there are some reported designs for isolated serial analog-to-digital converter (ADC) systems, the parallel implementation generally isn't considered due to the size and expense of multiple optoisolators. As an alternative, the design shown utilizes a single 24-pin hybrid component to obtain 10 bits of bidirectional transformer-isolated data transfer to implement a full 8-bit isolated parallel ADC *(Fig. 1)*.

The design was originally created to address a noise problem in a data-acquisition system that had too much digital breakthrough, raising the noise floor of the analog side. Overall, it occupies significantly less board space than the optoisolated scheme, and reduces total component cost.

The "NM1608 Octo-Isolator" contains eight buffered bidirectional data lines and two control lines (a device enable and direction control). The direction control function (DIRA) transfers the clock signal through the isolator, which automatically synchronizes the direction register. The device enable control (ENB) transmits the end of conversion (data ready) signal. Consequently, along with the eight data bits, the clock and data-ready bits also are transferred through the isolator.

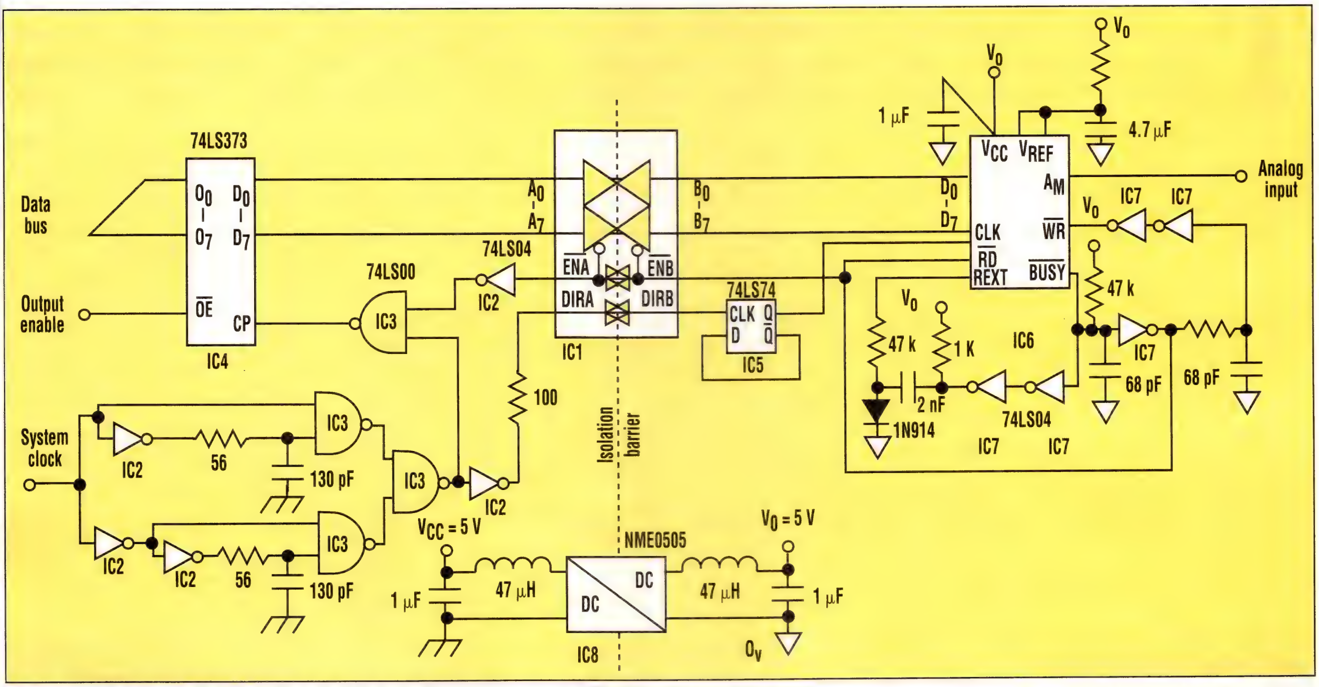
Passing a clock through a transformer isolator requires a narrow pulse train rather than a 50% duty-cycle train. The clock therefore is initially passed through an edge detector (R_1, R_2, C_1, C_2, IC2, and IC3), and then regenerated via a D-type flip-flop (IC5) after passing through the isolator.

In the circuit, a ZN448 ADC is set into continuous conversion mode. This continually cycles the ADC through conversions. When each conversion is complete, the Busy pin is driven high, feeding the enable pin of the MN1608 so that the data is automatically transferred on the next clock edge. The Busy signal is delayed to produce a pulse that's significantly wider than the clock edge pulse width. The data on the ADC data bus requires a maximum of 260 ns to settle. A delay on the signal to the WR pin, which begins the next conversion, is also used to ensure that data is settled (the WR pin internally resets the Busy signal low).

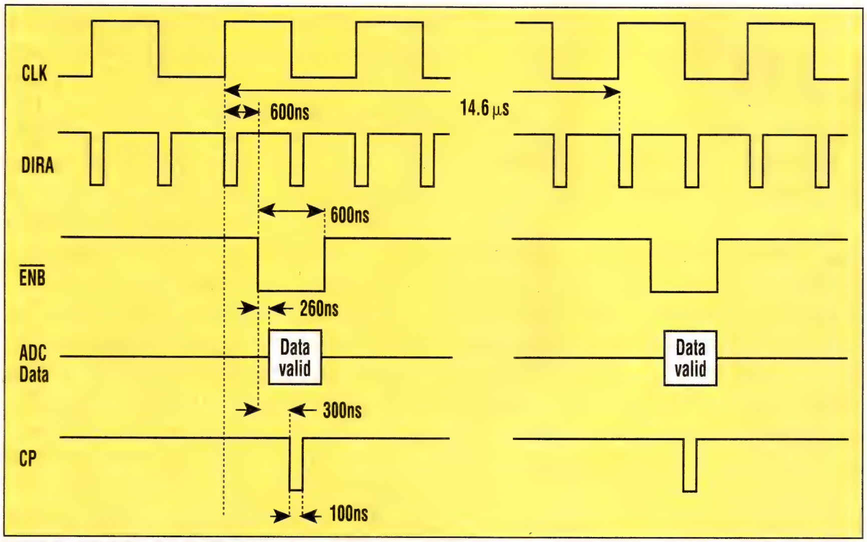
The enable pin and clock edge signals open the input latches at the data-bus interface (74LS373). These become transparent at the input and the data is transferred into the device (this condition only occurs with true data signals and not with tristate or mid-conversion data). The latch itself can be read asynchronously to the data-conversion system, because the last data conversion or current conversion result is available at all times in the latch.

The timings were all measured from the circuit with a 615-kHz clock *(Fig. 2)*. The data is always refreshed after nine clock cycles. This can immediately be improved by simply removing the D-type flip-flop after the NM1608, which thus makes the data available after every 4.5 clock cycles.

Because this scheme is suitable for parallel converters, the fastest throughput can be achieved with a



1. TO IMPLEMENT A FULL 8-BIT ISOLATED parallel ADC in a limited space, this design uses a single 24-pin hybrid component to obtain 10 bits of bidirectional transformer isolated data transfer.



2. TIMING MEASUREMENTS taken for the isolated parallel ADC were done with a 615-kHz clock.

flash converter and a faster clock. As a result, conversions could be available every clock cycle offering a minimum 9X speed increase on a similar serial scheme (the delays would have to be altered accordingly by changing the passive components and possibly the logic families used).☐

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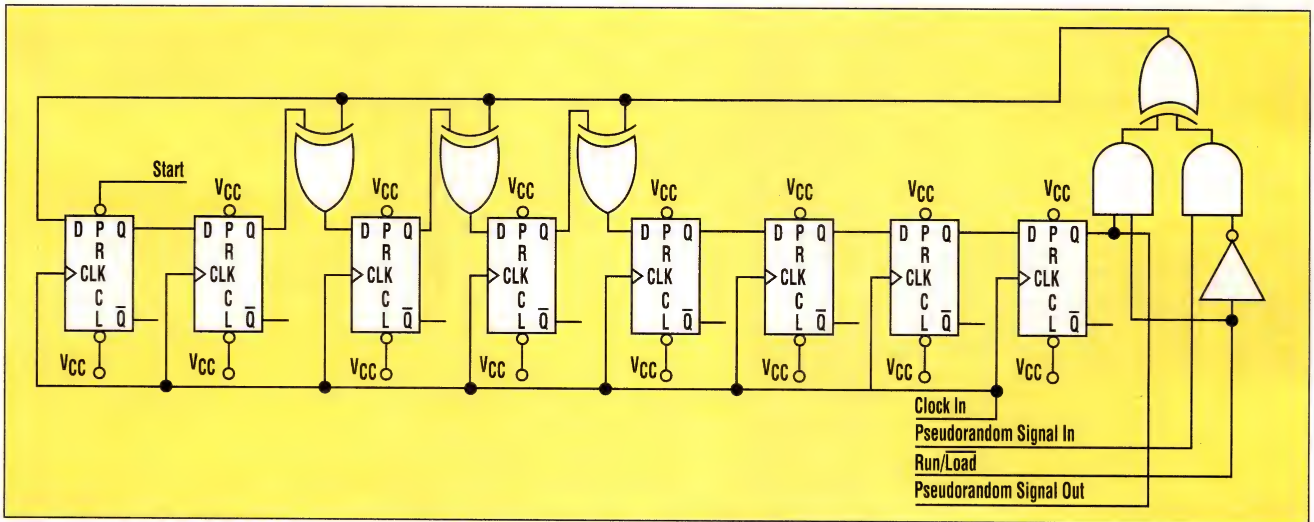
SYNCHRONIZE PRNG'S BIT STREAM, CLOCK

HANK WALLACE
Atlantic Quality Design Inc., 6425 Armindale Ave., Rural Hall, NC 27405;
(910) 377-2843, fax: (910) 377-9251.

The design of pseudorandom number generators (PRNGs) is easy and well documented. However, what if two PRNGs possessing the same feedback coefficients and clock rates have to be synchronized? Using the circuit shown, one PRNG can be synchronized to another reference PRNG's bit stream and clock *(see the figure)*. Of course, the clock and bit stream could be recovered from a transmission medium or carrier.

The circuit represents the usual PRNG with feedback taps selected to affect a suitable response. To synchronize this PRNG with another, Run/Load is set low and the two-input data selector breaks the feedback loop, inserting the reference pseudorandom bit stream (it's as-



SYNCHRONIZING one pseudorandom number generator's bit stream and clock with that of a reference PRNG is possible using this setup. Run/Load first is set low, then the two-input data selector breaks the feedback loop and inserts the reference pseudorandom bit stream. Once the target PRNG is loaded with as many bits as it has latches, Run/Load is set high, putting the PRNG in lock-step with the reference.

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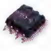

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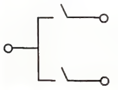

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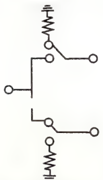

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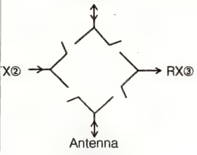

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sumed that the clock is either the same as that of the reference PRNG or is reconstructed using, say, a phase-locked loop). The target PRNG must be loaded with as many bits as it has latches (eight in the figure). When the PRNG is loaded, Run/Load is set high –and the PRNG walks in lock-step with the reference. The Start input to one of the latches will preset that latch because the PRNG doesn't start if all latches power up to a logic zero state.

The loading interval is not critical. If more than N bits for an N-bit PRNG are shifted in, the sync will still work. Therefore, it's not strictly necessary to count clock pulses while loading. A one-shot set for a period greater than N bits works fine for non-critical applications.

The circuit can be improved by adding a loss-of-sync detector, which is created by comparing the input and output bit streams. The comparison (suitably filtered) would drive the Run/Load input, allowing automatic sync acquisition.☐

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CIRCLE
523

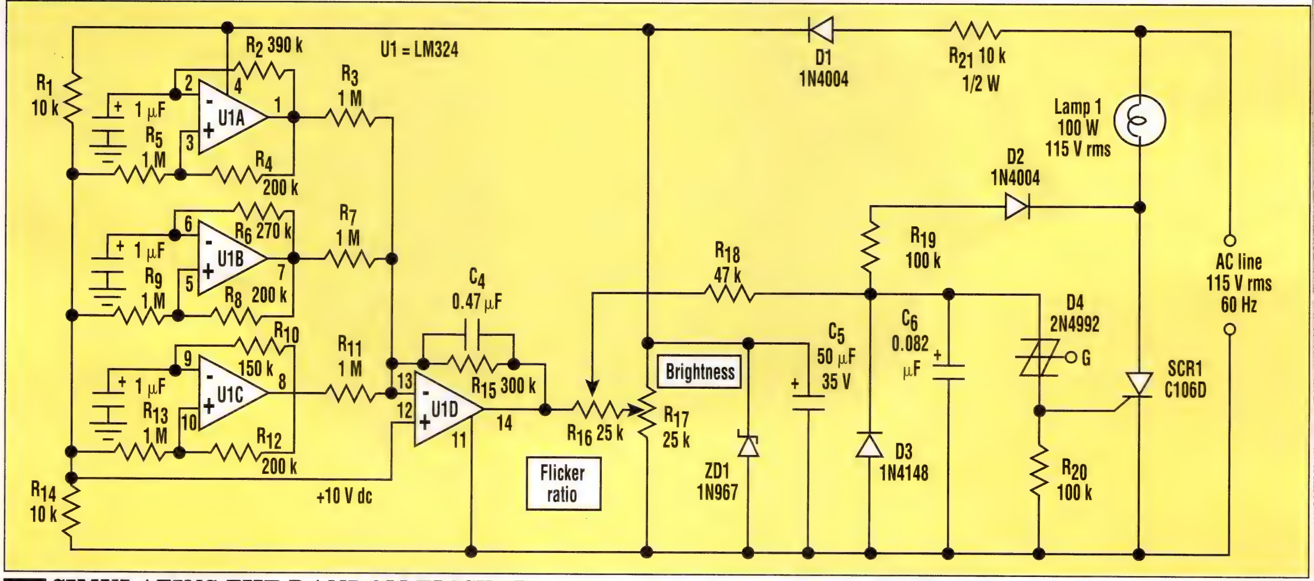
BUILD A DIMMER THAT FLICKERS

GEORGE ALTEMOSE
Pall Instrumentation Technology, 95 Oser Ave., Hauppauge, NY 11788;
(516) 273-0911, ext. 237, fax: (516) 951-2661.

The random flicker of an old-fashioned gas or kerosene flame can be simulated with this circuit, which has the ability to modulate the voltage delivered to light bulbs ranging up to 100 W *(see the figure)*. The average intensity and the flicker ratio can be adjusted with potentiometers.

The flickering dimmer consists of three independent, unsynchronized multivibrators, a summing and integration circuit, and a dimmer phase-control circuit. The three multivibrators, using three sections of the quad LM324, have oscillation periods of approximately 1 second, 0.7 seconds, and 0.4 seconds. The fourth section is used as a summing and integration circuit to sum the three square waves. The resulting voltage varies pseudorandomly from about 0 V to 20 V. This voltage is fed to the dimmer controller through the brightness potentiometer. The dimmer controller is a half-wave phase control that conducts only on the positive half-cycle. The conduction angle varies from approximately 0° to 180°. The brightness pot sets the average value, and the flicker ratio potentiometer determines the deviation from the average value.

It may be desirable to eliminate the flicker ratio potentiometer in some applications. In such cases, a fixed amount of flicker is determined to provide the optimum aesthetically pleasing effect.☐



SIMULATING THE RANDOM FLICKER of a gas or kerosene flame is possible with this circuit, which modulates the voltage supplied to a light bulb. Potentiometers can adjust the average intensity and flicker ratio.

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ELECTRONIC DESIGN QUICK LOOK

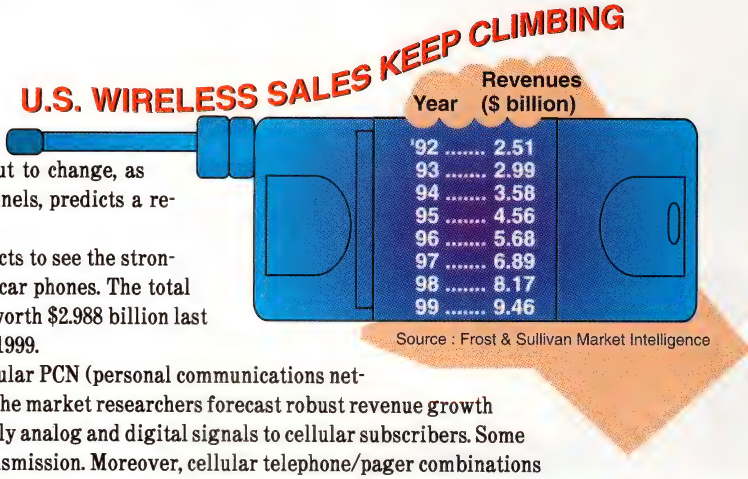
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Until now pagers and cellular phones have made the biggest inroads in sales and service industries. But that market picture is about to change, as sales to consumers increase through retail channels, predicts a recent study by Frost & Sullivan Market Intelligence.

The Mountain View, Calif., market research company expects to see the strongest growth in handheld portable phones that also work as car phones. The total U.S. market for wireless communication devices, which was worth $2.988 billion last year, should more than triple, amounting to $9.458 billion in 1999.

Among the developments to look for: lower cost, microcellular PCN (personal communications network) telephones and growth in numeric pagers. In addition, the market researchers forecast robust revenue growth in dual-mode cellular phones as network infrastructures supply analog and digital signals to cellular subscribers. Some models will provide for both cellular and satellite signal transmission. Moreover, cellular telephone/pager combinations are becoming popular with users who want to be able to screen their incoming calls before answering.


U.S. WIRELESS SALES KEEP CLIMBING

Year	Revenues ($ billion)
'92	2.51
93	2.99
94	3.58
95	4.56
96	5.68
97	6.89
98	8.17
99	9.46

Source : Frost & Sullivan Market Intelligence

TALES FROM A SKUNK WORKS

Most industrial age companies are organized into silos, that is, vertically. Unfortunately, products flow horizontally, across all the functions. This is why skunk works—smart, multidisciplined, independent, autonomous teams—can do so well in the right environment. Business frequently chooses trappings over substance. People can give every semblance of doing business, but really be pursuing hidden agendas for selfish gain. Such chicanery must be avoided for your skunk works to have a chance.

For worst-case examples, the government provides plenty—we've had some dillies in Oregon. One is "the PERS model." Bureaucrats love it because it is, so far, bulletproof. The governor or legislature sets up a board of directors with good connections to do business stuff (create jobs, bring money into the state, and so on).

That board then hires or sets up a separate company of presentable business people to investigate opportunities and administer details. The board makes the decisions and then the company analyzes, studies, reports, recommends, and so forth.

Sounds normal, you say? Perhaps. The trick is that, in reality, the board does whatever it (or their sponsors) feels like—usually pork barrel projects. The charade of business process holds up even under legal and media scrutiny. It is almost accepted that large sums of money will be wasted.

When public money vanishes into bad investments—a firm that operated for only two months caused $63 million to disappear—everyone is baffled. All the boxes have been checked, all is near legal, and fingers point in all directions. Criticism rarely gets beyond those who were diddling the details of the pseudo business.

Bureaucrats in government suck up tax money, and their equivalents in business destroy change agents. Kelly Johnson of Lockheed fame lamented in his book, *More Than My Share Of It All* (Smithsonian Institute Press, 1985), about how difficult it was to get others to use the skunk works model effectively.

At the beginning you need an unbiased, experienced outsider as coach and mentor to help you move to a skunk works. It can't be done with process, and you can't break outside the box from inside the box. If a manager's entire career is built on the control of hierarchical organizations, where does he learn to take risks, innovate, and empower? When new technologies emerge—and knowledge-based, self-managing teams are a new technology—this doesn't work. New methods and models are needed.

As an example, a friend had responsibility for a disastrous product. It was an unimportant minor component of a large system, designed quickly and poorly by a desperate subcontractor. The reject rate was almost total. His boss demanded a "tweak and test" procedure to remove the bottleneck. Unfortunately, that design never tested the same twice.

My friend said he could have done as well by weighing the units or flipping coins. Just as the test process can't fix bad designs, management technique can't establish effective skunk works. Content knowledge and experience is required for success.

John D. Trudel CMC is managing director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of High Tech with Low Risk. *To order, phone (503) 280-8547.*

EYE ON ISO 9000

Micron Custom Manufacturing Services Inc. has received certification to ISO 9001 for the board-level design, engineering, and manufacturing services of printed circuit assemblies at its Boise, Idaho, facility. Contact Micron Technology Inc., 8455 Westpark St., Boise, Idaho 83704-8366; (208) 368-2600. CIRCLE 460

An independent testing and engineering service organization, National Technical Systems has formed NTS Quality Services to help companies develop systems aimed at meeting such standards as ISO 9000. Among the programs offered are an executive briefing, training for personnel implementing standards, documentation review, internal auditor training, and trial assessment. For more information, contact Christine Briggs, NTS Quality Services, 533 Main St., Acton, MA 01720; (508) 263-2933; fax (508) 263-5734. CIRCLE 461

HOT PC PRODUCTS

As notebook computers become more powerful and versatile, with a corresponding drop in pricing, less RAM may come as standard in the computer. Apricorn supplies memory upgrade modules of up to 32 Mbytes of RAM for 28 brands of notebook computers. Users can install upgrades themselves, the company says. Contact Apricorn, 10670 Treena St., Suite 110, San Diego, CA 92131; (800) 458-5448 or (619) 271-4880. CIRCLE 462

QUICK REVIEWS

For developing power-based ICs, Meta-Software has a library of power subcircuits that, combined with the company's integrated CAE design tools, allows for switching regulators, pulse width modulators, inverters, and other building blocks for either board or IV-level designs. The circuit's electrical specifications can be automatically optimized to a given application. All the library subcircuits are supplied as HSpice files on floppy disks as standard Spice2G.6 files and are available on several BBSs. The library and technical research packet cost $50. Contact Kim Hailey or Dede Smith at Meta-Software Inc., 1300 White Oaks Rd., Campbell, CA 95008; (800) 346-5953; (408) 369-5400. CIRCLE 463

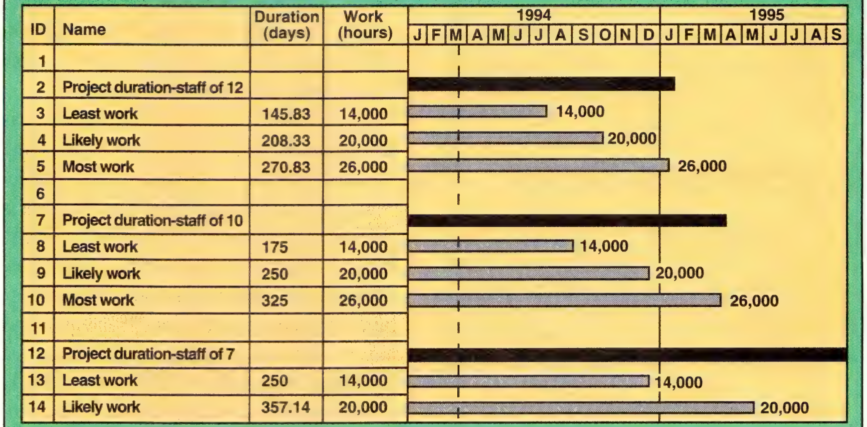
KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

Construction of the project's database relies on input from team members. But instead of supplying the project manager with duration information about each task, you supply work quantity information. As you identify tasks that you or others must perform, you estimate the work hours needed to complete the task—just one work quantity estimate for each task. And for each task, you provide commitment, predecessor, successor, and resource data. Using the database, the project manager computes the nominal duration of each task from commitment and work quantity; forms the task from the resource data. As he/she does so, you develop understanding of the interaction between work elements throughout the project. Information flows from team members to the database through group leaders. The project or program manager maintains the database and the quality of its information content. Team members provide accurate work quantity figures.

In the sample illustration *(see the figure)*, team members supplied data with a work quantity total of 20,000 hours. Starting with this initial figure, the project manager goes to work to earn his/her pay by determining this number's upper and lower limits.



ID	Name	Duration (days)	Work (hours)
1			
2	Project duration-staff of 12		
3	Least work	145.83	14,000
4	Likely work	208.33	20,000
5	Most work	270.83	26,000
6			
7	Project duration-staff of 10		
8	Least work	175	14,000
9	Likely work	250	20,000
10	Most work	325	26,000
11			
12	Project duration-staff of 7		
13	Least work	250	14,000
14	Likely work	357.14	20,000

Answering the question, "What functionality can be removed and what process risks can be taken to reduce work quantity?" helps find the lower work quantity limit. This is not an exercise in estimate reduction, but rather one of work reduction! A table forms that identifies each item of work that will not be done and the number of hours saved. Activity continues until reaching the point of diminishing returns while retaining sufficient functionality to sell the scaled-down product. This style of thought determines the lower limit on work quantity. In the example, the lower limit is 14,000 hours.

Next attention shifts to quantify the upper limit on total work quantity. To arrive at this figure, the project manager reviews my list of 40 things that go wrong on projects. It is not possible to predict which of the problems will strike or when they will occur, but it is possible to arrive at a work expansion figure that takes into account growth in work quantity due to problem discovery and problem correction. This awareness leads to the production or a work quantity figure greater than that supplied by team members. In the example, the upper limit 26,000 hours. The 6000-hour growth allows for encountering and solving up to six 1000-hour major problems. On average, 1000-hour problems take six months for resolution by one engineer. Now, the project manager works with the database under differing work quantity and staffing scenarios to compute the project's completion date, his work summarized in the figure. Of the nine alternatives, which would you select?

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MY VIEW

...Father knew best

BY FRANK J. BURGE
Director of Market Development for Electronic Design

My father had a thing about work and getting up early. When I was a young lad he would begin every one of our conversations with: "When I was your age . . ." At age 11 or so he suggested that I start delivering the weekly *Downtown Shopping News* with my wagon, which took three hours. I earned 90 cents.

The following winter Dad figured I was strong enough to handle the coal shovel and a pile of snow so he suggested I go door-to-door offering my services for 25 cents a sidewalk. Although I closed every deal, which I chalked up to superb selling, I now suspect the neighbors looked on it as entertainment, particularly since the shovel was bigger and heavier than I was. After the first week a neighbor, Mr. Hvizd, kindly offered me the use of his lightweight, regulation snow shovel. Shoveling was fun.

The next summer I gave up the *Shopping News* for *The Chicago American* route, a paid daily, which involved collections and tips. Even more fun than rolling the papers was tossing them from my bicycle with pinpoint accuracy. In the year I had that route, I broke only one window. My buddy Gootch Pazier rolled the tightest paper I had ever seen and could ride his bike at breakneck speeds without missing a porch toss. I've often wondered why paper rolling and tossing never became an Olympic sport because Gootch would have been an Olympic champion.

I must have been about 13 the summer my Dad decided I needed to get close to nature. So he got Joe O'Connell and me jobs at a nursery. After punching in at 7 am we were assigned to the manure pile and shoveled manure into the endless rows of flower beds for what seemed like days. Toward the end of the day we were transferred to another section of the nursery to pick weeds. Now the weeds were bigger than the flowers so every time we grabbed a handful of weeds we'd also come up with a bunch of flowers. When the weed warden strolled by to inspect our work he flew into a rage and fired us. We'd worked 12 hours and made $4.20 each. Joe figured we were lucky we flunked weeding or the warden would have kept us there all night. That evening I asked my Dad not to pencil us in for any more gardening assignments.

By the time we were in college O'Connell and some of my other buddies were working summers as boilermaker's helpers and I had landed work as an apprentice sheet-metal worker. One summer we had a job in the steel mill and I'd meet the crew at the saloon across from the mill at 6:45 am, which meant leaving home at 5:30 am. Tough duty, particularly if I had been partying the night before. But my Dad made certain I got up on time, his 4:45 am wakeup a reminder that I couldn't party all night and expect to sleep all day. Besides he was convinced getting up early was healthy, something to do with the morning air. Anyway I'd arrive at the saloon across from the mill at 6:45 am and watch as the old timers tossed down two shots and two beers before starting the work day. Guess the morning air wasn't enough to get them kick started. But that summer working at the mills was a wonderful summer thanks to Ziggie, Ski, Johnny and the sheet metal gang. But that was a long time ago.

We spent last Christmas with our daughter's family in Northern Wisconsin and one evening I was looking out at the snow with my 10-year-old grandson Robby. And then it happened: "You know, when I was your age I was out shoveling . . ." but before I could finish I caught myself. Robby asked what I was talking about? "Oh nothing," I replied, figuring he'd never understand. But there was a time when father knew best.

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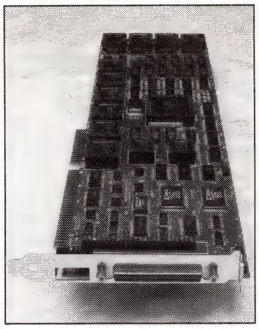

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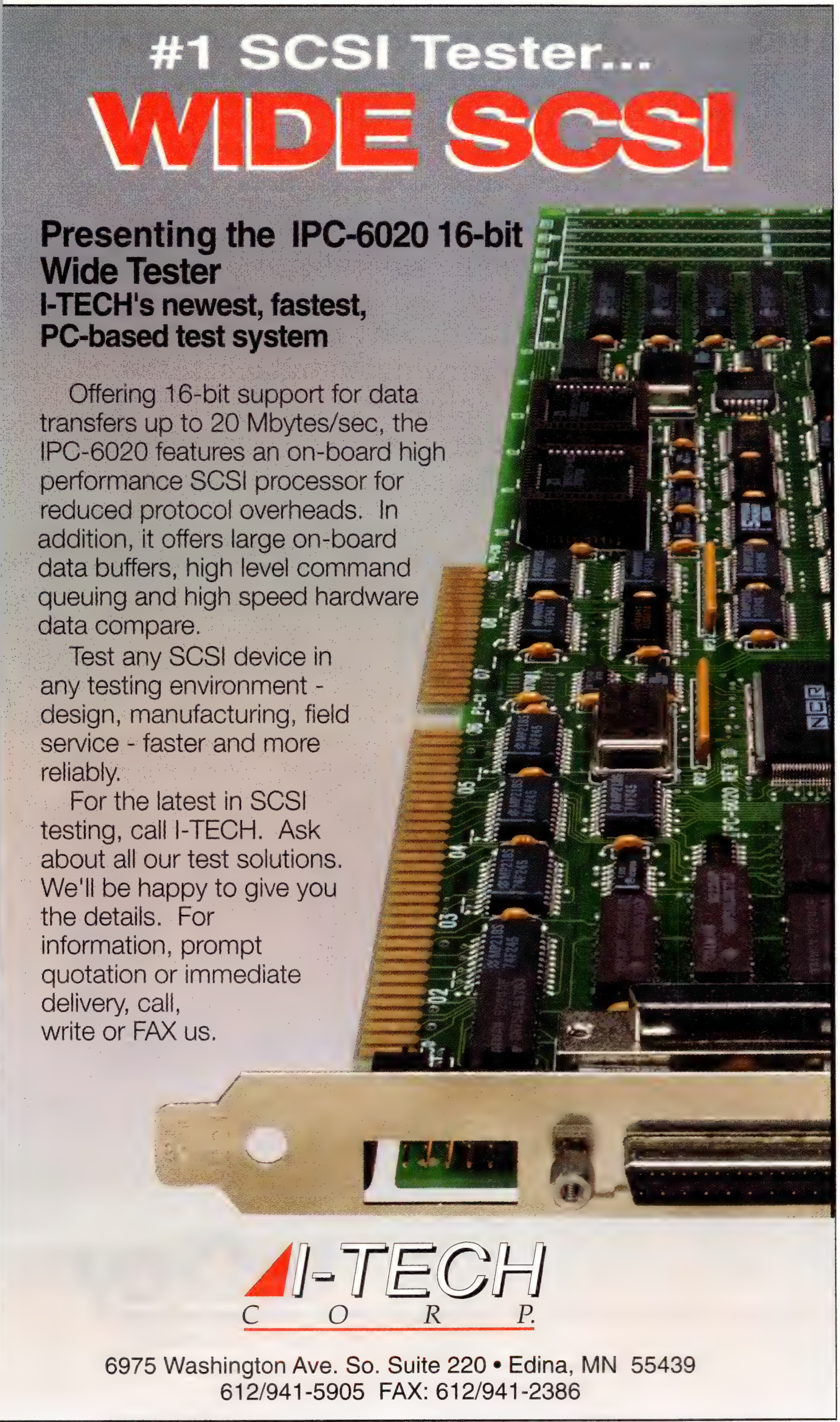

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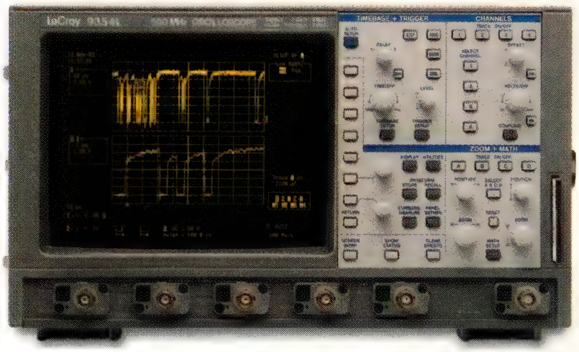

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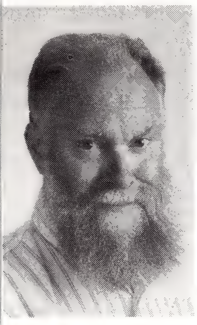
PEASE PORRIDGE

WHAT'S ALL THIS APPLES & ORANGES STUFF, ANYHOW?

Yes, recently I was invited to take yet another "Training Course," following in the path of great successes such as Taguchi Methods, Fuzzy Logic, and Time Management. But why would this course on basic accounting and economics be called "Apples and Oranges?" Because, the course's leader explained, if one person has apples and another person has oranges, the only way to quantify the sum total of the two fruits is their value in dollars. So we quickly dropped the old aphorism that "you can't compare apples and oranges," and started talking about dollars.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

We soon agreed that it was a good idea for our company to be profitable, and that all of us employees ought to be aware of how to improve profitability. But, how is the profit to be measured—how do we do the accounting? We started out with a little game from Learning Methods International, Box 50, S-230-42 Tygelsjo, Sweden. The purpose of the game is to teach you which expenditures of a manufacturing plant are used to compute the profits, and how the costs and expenses and assets are added and subtracted and divided to compute the Return On Investment. Michael, the leader, gave us an explanation of how the "game" is supposed to run—a discussion of how this little hypothetical "factory" buys raw materials and adds labor to accomplish the manufacturing of Widgets. Then the Widgets were put into "Finished Goods" to await customer orders. Over the course of a year, this factory was able to show a good operating profit. But after expenses for interest and taxes, the after-tax profit was only $2 million—not a very good profit on $80 million of sales.

Michael suggested that we go back and recompute the profits if we went back and followed a different game plan: We should pay off $20 million of our liabilities (bank loans) with some of our cash. Sure enough, at the end of the year, the net profits looked considerably better, about $3 million. Further, he suggested that we should not keep a lot of our finished products in Finished Goods (or, "Box Stock", as we call it at National), but we might plan to just build our Widgets to meet customer orders. We could save a lot of money by not having a 3-month stock of expensive assembled parts waiting around for customer orders. FURTHER, we could save additional money by not buying our raw materials from just any cheap suppliers, but rather by choosing a "small number of very reliable suppliers" that we could trust to ship us our raw materials on a JIT (Just-In-Time) basis. This saves more money by not having raw materials sitting in our storehouse for a long time. Altogether, after we ran the numbers through the exercise, our new lean, mean company had made $6 million of net profit. Wasn't that a lot better, asked Michael?

I spoke up, "HELL, NO! The only reason we were able to save $4 million in interest was because this whole scenario was set up badly. In the base example, the company treasurer sat on an average of $51 million of cash, and never even put it in the bank to earn daily interest. The only way we could show an improvement of $4 million on interest was to ignore the fact that the treasurer had wasted $8 or $10 million in interest he could have earned. Even in the second scenario, there was $3 or $4 million left lying on the table due to the treasurer's ignorance and/or incompetence.

It's absurd to argue that one plan shows superiority if it's only compared to a Straw Man." (As you can see, I am not a big fan of Straw Man comparisons....) So the lecturer immediately spotted me as a troublemaker. "Well, yes, you are right, but we just have to follow these examples and procedures for accounting, which are, of course, simplified."

Next I complained that if you order your raw materials from "a limited number of highly reliable suppliers" for the purpose of getting "JIT delivery," you should honestly expect to pay more for that. I've heard that half the trucks in Tokyo are driving around in circles, half-empty, wasting time so they can show up at JUST the right minute, neither late nor early.

This might make your assembly operations simpler, but that JIT service is NOT free, and not necessarily cheap. Somewhere, somehow, you will pay for it. Further, one traffic jam, one flat tire, and your production line goes down. "Yes, but we are just following our guidelines, which are of course simplified..."

Later, I pointed out, after the game had been played for three years of financial analysis, "Isn't it kind of stupid to make only $80 million a year of these Widgets? What the heck is going on? In most cases, if you spent another $1 million to hire some better salesmen, you could sell a lot MORE than $80 million, and the increased profits would more than pay for the cost of sales." NOW, I must admit, in a hypothetical example, maybe we can't be more specific on what a Widget really is. So if a "Widget" is a kind of commodity such that, no matter how many you have, no matter how

PEASE PORRIDGE

smart the salesmen are, they could not sell more than the customer was planning to buy—then we should not insist on hiring better salesmen. But otherwise, we would be remiss if we didn't study that possibility. The Instructor agreed that, in some cases, expanding sales is indeed the right thing to do, but there was no room to show that in this simplified example.

After Michael begged me not to be such a disruptive influence during the class, I met with him during lunch hour. I pointed out that in his "simplified" example, he claimed that he was able to sell the same $80 million of Widgets by manufacturing them on a Just-In-Time basis. But at NSC, we often found customers who WANTED to buy a product from stock RIGHT AWAY, but if we had nothing in stock, they would have to buy elsewhere.

So IF you're in a business in which you're SURE that nobody will buy MORE parts just because they are on the shelf, and you're SURE nobody will buy LESS just because the parts are NOT on the shelf, well, go ahead and do your JIT manufacturing. But I warned him that this OVERSIMPLIFICATION was NOT necessarily good for business, NOT good for profits, and NOT valid for improving ROI. He conceded that my arguments might have some truth—but there was no room for them in this simplified analysis.

One of the other students said, "Well, Bob, you may not like the simplified stuff in this course, but it sure got you thinking." I replied that I had been thinking about this very seriously for several years, and I already figured out some of the weaknesses of JIT manufacturing. Hearing this guy just preaching oversimplified economics got me so ticked off that I was going to do something about correcting this problem. And even though *your* company may not make the same kind of products as mine, you probably face the same kinds of issues.

Where I work, I'm often concerned about how we can avoid a complaint from a prospective customer: "How can I design in your parts right away if your samples are only available on a three-week delivery from Malacca?" So I worked pretty hard with our planners to maximize our ability to ship evaluation samples overnight, or in 1 or 2 days. But I have to fight with some guys who think that keeping our samples in the low-rent district of Timbuktu is a great way to save money. I certainly don't need a training course to simplify things to the point where people think that the cheapest costs are always the right solution.

Furthermore, I do get calls like—"After I get your new parts designed in, how can I go into pilot production if the availability is 6 weeks?" I point out to them that while we may not necessarily have these parts in stock, we have distributors who do a pretty good job of keeping at least small or medium quantities in stock, so you can order them and get prompt delivery. We want to keep a lean (but not *zero*) inventory.

Now, if a guy complains "I ordered the ICs for my first production run; then the product got HOT and I wanted to double my production run—but the availability of parts was not good. What do I do now?" I've been arguing for years that we should make sure our sole-sourced parts, our proprietary ICs, and, for that matter, any of our products that have a decent volume and good profitability are kept in stock in some reasonable quantity. The alternative is to tell your customers, "We can't help you; you will have to design in our competitor's parts." So when I heard this nincompoop at the training session arguing that we should show a better ROI by only selling Widgets to people who can place orders well in advance of when they needed them, I decided to start chomping my teeth into peoples' ankles to straighten out this oversimplified economic foolishness.

One copy of my first draft went right to our Chief Executive Officer, Gil Amelio, and I have also brought it to the attention of *lots* of other people in sales, marketing, and planning areas. These guys have given me much support and encouragement. Maybe Michael doesn't want any loose cannons in his lecture room, but in the real world, if somebody else doesn't complain about stupid, oversimplified strategies, then it becomes my job. Go ahead, tell me that I'm a loose cannon. We all already knew that. Even a loose cannon can do some good if it sweeps away cobwebs. Maybe I can't tell the difference between apples and oranges, but I can tell the difference between bad economic theory, OVERSIMPLIFICATION, and the real world.

Now, speaking of oversimplification, when I propose keeping these new proprietary or sole-sourced parts in stock, I shouldn't imply that it's *easy* to do. Murphy's Law says that as soon as I see a part selling with good volume and I put a fat amount of them in stock, then people will stop buying them. If I put the expensive one in stock, people will want to buy the cheap ones (and vice-versa); if I stock the mini-DIPs, engineers will specify the surface-mount versions. So if I indicated that keeping the right balance of parts in stock would be easy, I must apologize for my own oversimplification.

We have to try to anticipate our customers' ordering patterns. We have to try to keep a reasonable bank of good, tested dice, so no matter which packages the customers ask for, we can assemble the right ones quickly. To do this promptly may require an agile, fast-response assembly group. This may cost a little more, but the advantages may well be worth it in terms of being able to respond and fulfill customer needs.

Also, that doesn't mean that we just have to keep lots of parts in our store rooms. If one distributor is keeping one part in stock, and another is stocking another part, then we may not have to keep many of those parts around at all. But we have to keep a few around for quick sampling.

I talked with some of the guys who designed the original three-day comprehensive lecture about reality and economics. They were surprised to see how unrealistic and badly oversimplified the economic studies became when they were pared down to a one-day course. They agreed it was probably time to see what we could do to restore some reality to that little course. I sent in five scribbled pages of my suggestions on how to restore some of the redeeming factors. I also invited the accountants who really know what's important in fiscal mat-

PEASE PORRIDGE

ers to add comments about things I didn't notice, or am not very knowledgeable about. Maybe next year, the "Apples and Oranges" course will not only be "training," but will really *educate* us on how to make our company more profitable! The best way for all you managers out there (and other workers, too) to please *your* customers may involve *thinking*—NOT just referring to some old obsolete formula or cookbook.

All for now. / Comments invited!
RAP Robert A. Pease / Engineer

Address:
Mail Stop D2597A
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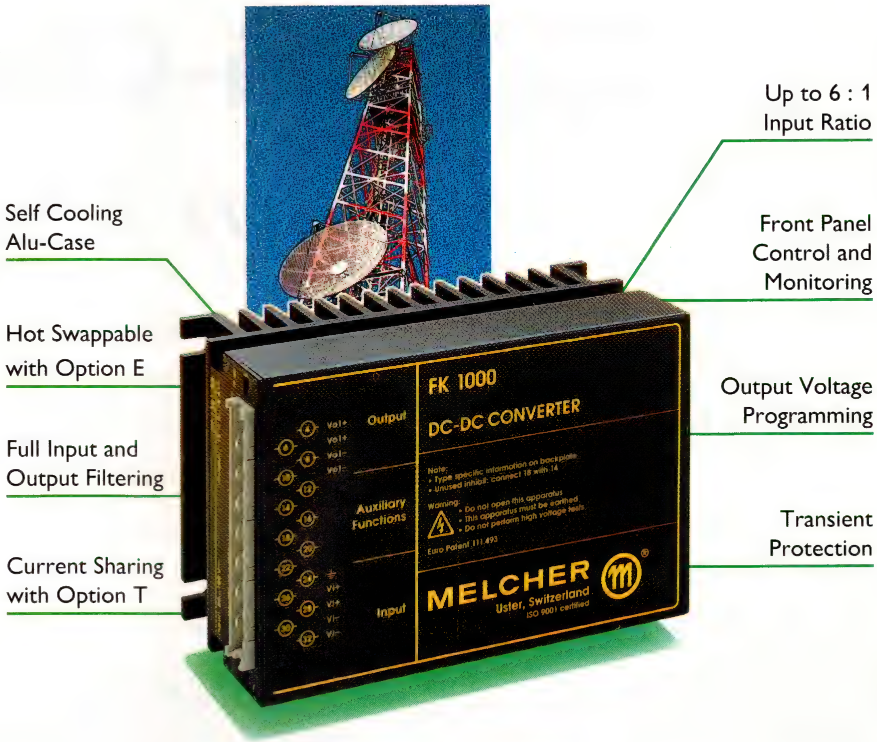
P.O. Box 58090
Santa Clara, CA 95052-8090

p.s. Mark Levi, who was involved in the design of the original Apples and Oranges course, and who helped me a lot in getting this column into good shape, suggested I read a book: *The Goal*, by Eliyahu M. Goldratt and Jeff Cox. This is written in the form of a novel about a guy who is trying to run a manufacturing plant in the midst of *all sorts of* trouble. His customers are screaming about late delivery, his workers are setting contradictory rules, his most efficient machines are being misused, and his boss is threatening him.

Meanwhile the bean counters tell him everything he does to improve the situation is wrong. A very stressful job—trying to bring in a few more dollars to show his boss why the plant should not be shut down. This is a COMPLETE antithesis of Apples and Oranges, that Pollyanna-ish waste of time. However, Mr. Goldratt doesn't gratuitously overcomplicate things—he sets reasonable examples and covers one or two problems at a time. Good thinking, good writing. The book was published in 1986 by North River Press, Box 241, Croton-on-Hudson, NY 10520.

You can order by calling (914) 941-7175. Price is about $19.95. Bravo to a good story-teller, explaining how the real world is horribly different from those orderly, sterile optimization situations you learn about in school. —RAP

More than just a Power Component



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Input [V]	Single Output	Dual Output	Outputs [V_{DC}]
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28…140 V_{DC}	CK 1000	CK 2000	Dual: 12/12; 15/15; 24/24
44…220 V_{DC}	DK 1000	DK 2000	resp.: ± 12; ±15; ±24
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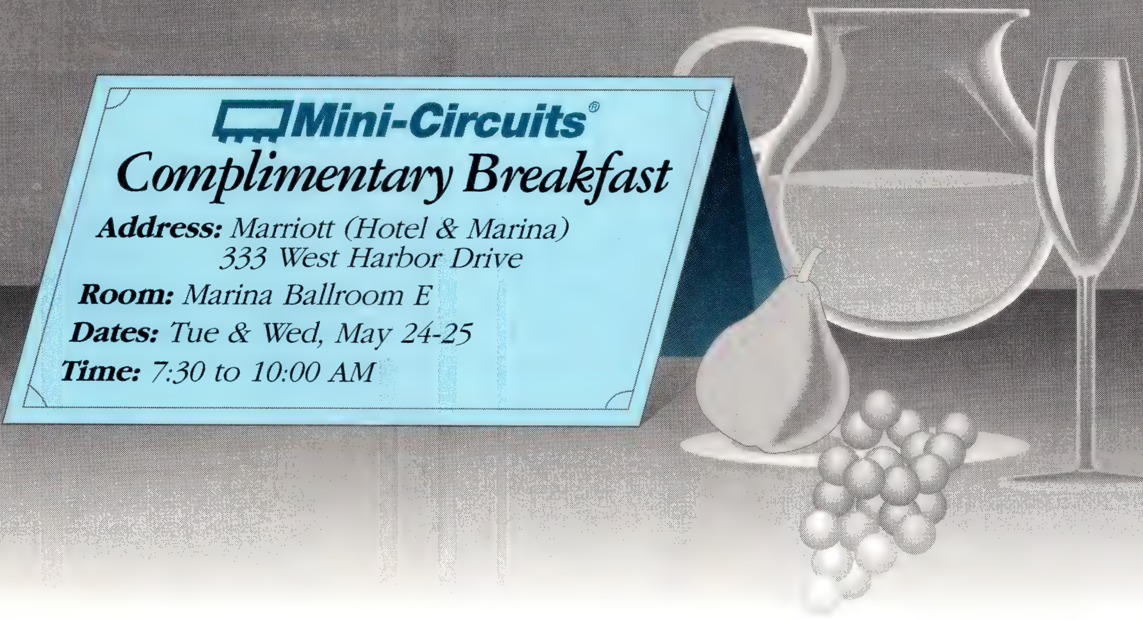

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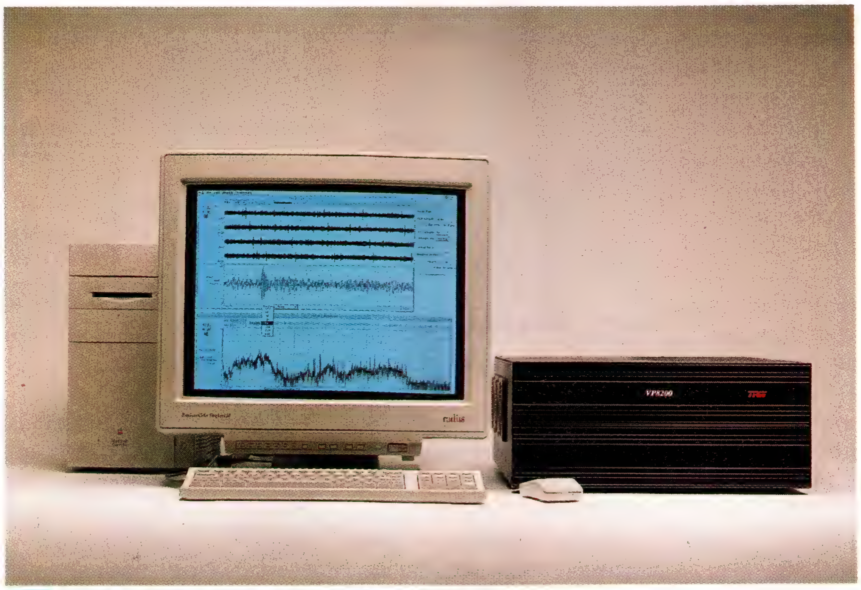


1. IN ONE COMPACT CHASSIS, the VP8000 supplies stimulus, response, and analysis functions. A massive 64-Mbyte cache memory is available.

STIMULUS, RESPONSE, AND ANALYSIS IN ONE HIGHLY INTEGRATED SYSTEM MAKE DESIGN VERIFICATION FASTER AND LESS EXPENSIVE.

ONE-BOX TEST SYSTEM DOES IT ALL

JOHN NOVELLINO

At times it seems a high-performance test setup can be just as complex as the design it's meant to evaluate. The engineer might have to assemble several instruments to create a test system, run multiple test protocols to collect enough data, and maybe even change the test hardware to run a different set of protocols. At that point, the measurement data may have to be moved to a computational platform for analysis.

Needless to say, one instrument that could deliver the stimulus, acquire the response, and then analyze the results would be quite a boon to designers. Engineers at ESL Inc., a TRW company, were thinking on those lines as they developed the VP8000, ESL's first commercial test and measurement product after decades of supplying government reconnaissance and intelligence systems. The VP8000 relies heavily on the data-collection, processing, and analysis technologies used in those government products.

ESL considers the VP8000 to be a new class of design verification and test equipment because it fully integrates the features of a computer with the measurement power of instrumentation. Although a number of options and choices are available, a complete system includes a signal generator, a data-acquisition module, a playback module, and an analyzer. Such a level of integration allows ESL to seamlessly combine a massive memory (up to 64 Mbytes) and workstation with the test setup's stimulus and response functions. Consequently, designers can employ computer-resident simulation inputs, correlate stimulus and response, and execute and analyze long test runs from one platform *(Fig. 1)*.

The VP8000's modular architecture allows customers to configure a factory-customized instrument based on the desired input and output ports, memory depth, and analysis capability. ESL then incorporates custom or commercial cards into the system as needed.

With application software, users can create virtual instruments to make the measurements. Customers are able to choose between the Macintosh Quadra (using a NuBus interface) and a Unix-based workstation (with a SCSI interface) for the system host. ESL says that other hosts will be supported in the future. Any processing software on the host has full access to the cache memory at a sustained speed greater than 1 Mbyte/s.

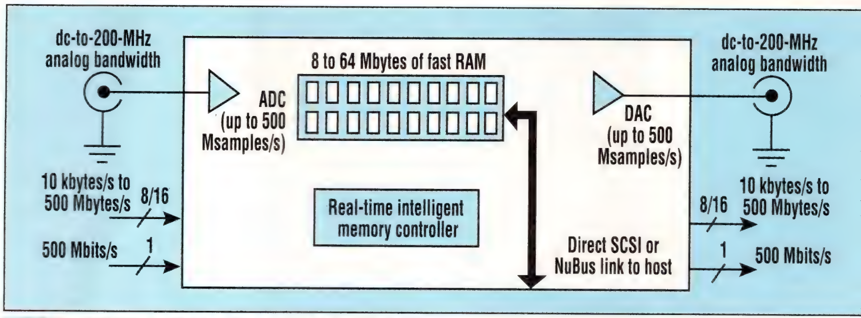
Customers can opt to have a system configured with two, one, or no inputs and outputs *(Fig. 2)*. I/O choices include 12 bits at 25 Msamples/s, 8 bits at either 250 or 500 Msamples/s, 8- or 16-bit parallel digital ports at 250 or 500 Mbytes/s, and 500-Mbit/s serial ports. Signal conditioning available includes 200-MHz gain control and antialias filtering.

The VP8000's maximum bandwidth is 200 MHz, while throughput can be 500 or 250 Mbytes/s. Cache memory can range from 8 to 64 Mbytes in increments of 8 Mbytes. An intuitive user interface employs point-and-click menu bars and windows.

The system can be configured for coherent input of two identically formatted channels or a switched input of two differently formatted channels. The same holds true for the output.

CABLING ELIMINATED

One key to the VP8000 is that it eliminates the need to cable together multiple instruments. The input side of the system acts as a digital storage oscilloscope, and the output side performs the jobs of signal synthesizers, function generators, pulse generators, digital data generators, and arbitrary waveform generators.


dc-to-200-MHz analog bandwidth
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ADC (up to 500 Msamples/s)
DAC (up to 500 Msamples/s)
dc-to-200-MHz analog bandwidth
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8/16
500 Mbits/s
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Real-time intelligent memory controller
Direct SCSI or NuBus link to host
8/16
10 kbytes/s to 500 Mbytes/s
1
500 Mbits/s

2. CUSTOMERS CAN SELECT from a wide range of I/O capabilities in the VP8000. Internal components communicate over a proprietary bus.

All components communicate with each other over ESL's proprietary bus. The hardware is based on a proprietary chip set that facilitates the formatting and routing of high-speed digital data. The VP8000's core technology was developed in 1990 for government use in collecting and analyzing large segments of wideband signals with tightly-integrated software.

The extremely large cache memory will allow most users to capture all of the data needed in one test run. The measurements then can be analyzed immediately by system-resident software. Users can break up the memory into multiple independent segments for either signal capture or generation. The memory can be randomly addressed by the different software applications. Data within the cache memory can be transferred to disk files on the workstation host for archiving.

Four software packages are currently available with the VP8000. The first, View IDAP, supplies display functions to control signal acquisition and generation, and it comes with the base system. The Waveform Analyzer package creates a time-domain display similar to that of a digital scope. Users can browse through the cache memory, zoom in time and frequency, perform measurements, and cut and paste segments from the cache memory to disk files.

The Fourier Analyzer software provides frequency-domain displays and measurements, with a 200-MHz instantaneous bandwidth and weighting, averaging, hold, and zoom functions. Finally, the Development Environment package offers a library of VP8000 hardware controllers and drivers for inclusion in the user's custom software applications. Compilers are supplied where appropriate.

In addition, the VP8000's data files are compatible with popular commercial data-analysis software, such as Mathematica and Matlab. The data can be used by the software, and the software can create data for the system. As a result, users are able to customize their data- and signal-processing techniques.

ESL will initially target designers developing telecommunications and medical instrumentation as prime candidates for the VP8000, according to John Ammirati, marketing manager for TRW's Business Intelligence Systems. "The communications and medical instrumentation markets demand exacting performance standards that call for definitive testing over a full operational range," says Ammirati. "The VP8000 links the computer to the real world by providing access to real signals, not just numbers, so simulation and testing are more accurate and have a bigger impact on product quality." ☐

PRICE AND AVAILABILITY

Prices of VP8000 systems range from $50,000 to $90,000, depending on the configuration and specifications selected. A sample system, which includes an 8-bit, 250-Msample/s digitizer; 32 Mbytes of memory; and the View IDAP and Waveform Analysis software, costs $55,000. Production quantities will be available next month, with deliveries estimated at 60 days after receipt of an order.

ESL Inc., 495 Java Dr., P.O. Box 3510, Sunnyvale, CA 94088-3510; (408) 752-2423.

CIRCLE 511

HOW VALUABLE?	CIRCLE
HIGHLY	533
MODERATELY	534
SLIGHTLY	535

PRODUCTS NEWSLETTER

CONTROLLERS HAVE 40-MBYTE/S BANDWIDTH

High-end hard-disk drives will profit from the AIC-8300 family of disk controllers from Adaptec Inc., Milpitas, Calif. The ICs offer a 16-bit 40-Mbyte/s buffer bandwidth. Both hardware and software error correction is implemented. In addition, a byte-wide three-way Reed-Solomon error-correction code also adds to the performance improvement. Other features include automated data-flow management and automatic read and write cache support. The family builds on the previous generation AIC-8200 family of controllers. The 8370 operates through the Fast IDE interface, modes 3 and 4. It's also compatible with ATA modes 0 through 2. The 8320, for SCSI-based drives, is designed with a fully programmable RAM sequencer. An evaluation board is available, as well as a series of programming and development. Samples of either chip cost $20. The 8370 is sampling now, with production beginning in the late summer or fall. The 8320 will sample in June, with production starting three to six months later. For more information, call Adaptec at (408) 945-8600. *RN*

CIRCLE 945

PCMCIA DEVELOPMENT KIT CUTS TIME TO MARKET

Designers will have an easier time building PCMCIA-based I/O and memory cards using the StarCard II frameless card kit. The prototype card is designed with two surface-mount connectors, stainless-steel snap covers, and a shielded cable. The frameless design frees up extra space on the pc board. The kit, developed by ITT Canon, Santa Ana, Calif., will reduce the time and cost of manufacturing cards and bringing them to market. The self-aligning connector eliminates the fixture and alignment problems that can hinder the manufacturing process. As a result, manufacturers don't have to physically remove the card's pc board from the assembly line to incorporate the PCMCIA connectors onto the card. A high-reliability pin-and-socket design ensures electrical contact between the connector pin and the joining socket. The snap-together cover eliminates the need for adhesives during manufacturing, which improves the speed and cleanliness of the production process. For more information on the StarCard II, call ITT Canon at (714) 261-5300. *RN*

CIRCLE 946

DEVICE SHUTS DOWN PC DISPLAY

Electric bills can be reduced using the Green Keeper, from B&B Electronics, Ottawa, Ill., which automatically shuts down a computer's display. The device is similar to a screen blanker, except that it turns off the power, rather than just blank the display. The rest of the computer remains on. It connects in series with the keyboard of a PC, and the display gets plugged into the Green Keeper. The software, which runs under either DOS or Windows, monitors the computer's activity, and shuts off the display after a user-specified period of inactivity. A touch of the keyboard or mouse brings the display back to life. The inactivity period can be set to different intervals for different parts of the day. For example, it could be set to 15 min. during business hours, 1 min. during lunch time, and 1 min. during non-business hours and weekends. Up to nine different time-outs can be set. The Green Keeper is priced at $69.95. For more information, contact B&B Electronics at (815) 434-0846. *RN*

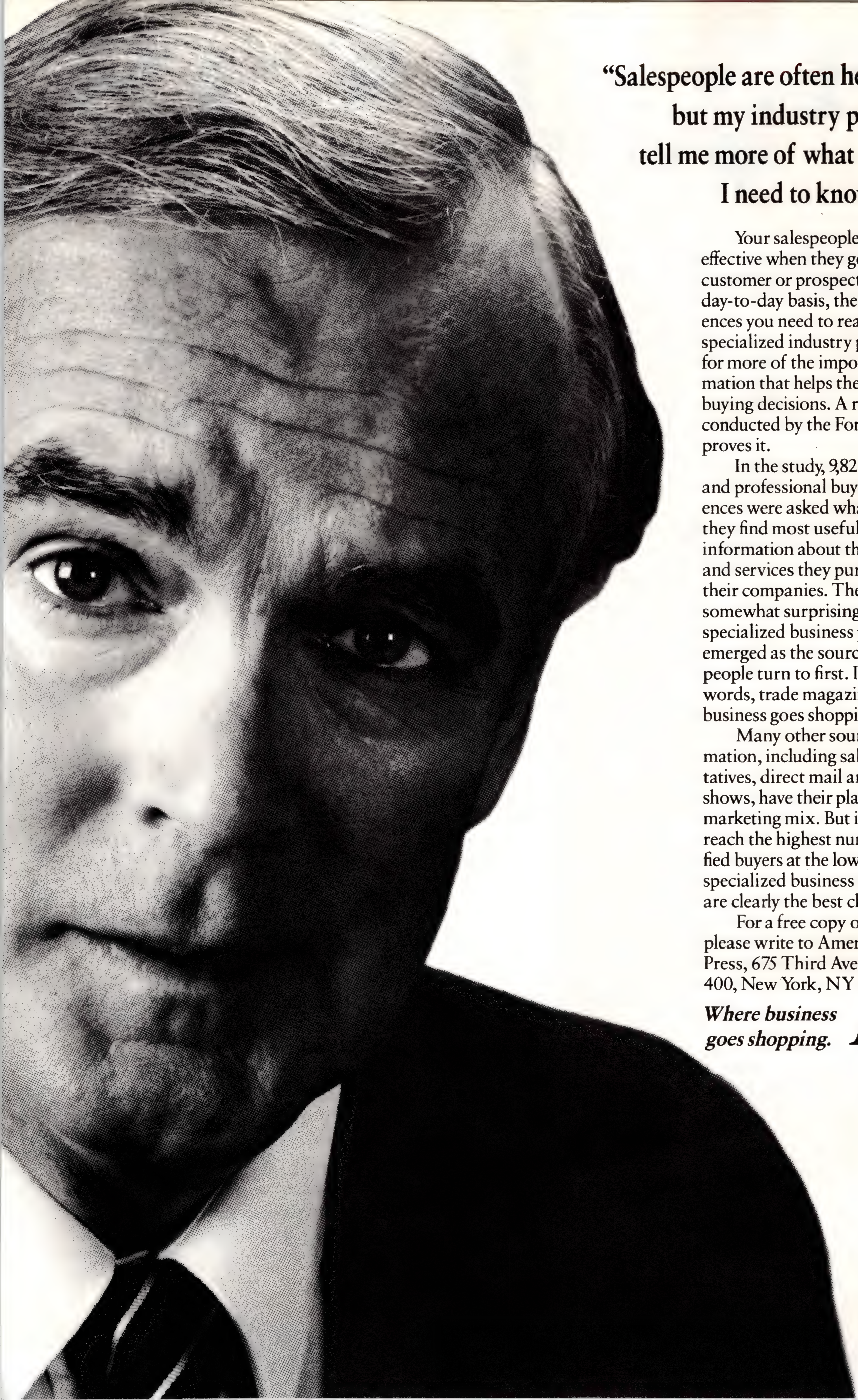
CIRCLE 947

PROVEN VERILOG CLONE COSTS LESS THAN $1000

VeriWell, a PC-based Verilog simulator clone from Wellspring Solutions Inc., Sutton, Mass., costs less than $1000. The VeriWell simulator, which runs on virtually any DOS-based PC, has been proven in customer designs at companies like Raytheon Semiconductor. This success has prompted the company to add support for Macintosh and Sparc platforms. VeriWell/Sparc and VeriWell/MAC have the same capabilities as the company's existing simulator. The VeriWell products are compatible with the Cadence Verilog-XL simulator, so entire design hierarchies can be moved between the two tools without changing the command or input files. The VeriWell/Sparc and VeriWell/MAC products are available now for $2995 and $1495, respectively. The existing VeriWell/386 and VeriWell/PC (16-bit implementation) versions for the personal computer go for $995 and $495. A waveform viewer called Wellspring Waves costs $449. Call (800) 837-4935 or (508) 865-7271. *LM*

CIRCLE 948

Edited by Clifford Meth



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Your salespeople can be effective when they get to see a customer or prospect. But, on a day-to-day basis, the buying influences you need to reach turn to specialized industry publications for more of the important information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, proves it.

In the study, 9,823 business and professional buying influences were asked what sources they find most useful in providing information about the products and services they purchase for their companies. The results were somewhat surprising. Overall, specialized business publications emerged as the source business people turn to first. In other words, trade magazines are wher business goes shopping.

Many other sources of information, including sales representatives, direct mail and trade shows, have their place in the tota marketing mix. But if you want t reach the highest number of qualified buyers at the lowest cost, specialized business publications are clearly the best choice.

For a free copy of the study, please write to American Busines Press, 675 Third Avenue, Suite 400, New York, NY 10017.

Where business goes shopping. **ABP**

FAST ETHERNET CHIP LETS DATA MOVE AT 100 MBITS/S

Packing a dual-speed CSMA/CD engine that runs at 10 or 100 Mbits/s, the SMC91C100 reduces system complexity to just one controller chip, some buffer memory, and the cable interface. The dual data rates allow the chip to also serve as a bridge between the two networks, receiving data at one speed, and transmitting it at the other. The 100-Mbit/s Fast Ethernet standard allows for two cabling options—100Base-X, which employs two pairs of category 5 cable, and 4T+, which employs four pairs of category 3 cable. Both formats employ 100-Mbits/s data rates using the standard Ethernet CSMA/CD protocol. The controller has a 32-bit-wide interface to the packet buffer memory and a 32- or 16-bit interface to the host system bus. In addition, the controller provides synchronous, asynchronous, or burst DMA interface options to the host systems to maximize data transfers between the controller and host memory. Up to 128 kbytes of external memory can be addressed by the 91C100, which uses a flat memory-management unit architecture with symmetric transmit and receive structures and queues. The controller also includes transparent arbitration, so systems can be implemented with a slave sequential-access architecture.

The 91C100 is software compatible with the company's SMC9000 Ethernet controllers. The 100BaseT (4T+) implementation uses the same cable lengths as 10BaseT—about 100 m—and the same star topology. However the network span is limited to 240 m. It can also use four pairs of telephone-grade (or better) twisted pairs employing a three-level signalling scheme. The 100BaseX implementation uses two pairs of category 5 cabling, and a protocol based on the copper digital data interface (ANSI X3T9.5). That scheme sends 125 Mbits/s over the cables (100 Mbits/s effective data rate).

To interface the 91C100 to the network, the 83C694C provides a 10-Mbit/s interface for 10BaseT systems, while a forthcoming chip, the PHY100 provides the tie-in to the 100-Mbit/s cabling.

Housed in a 208-lead PQFP, the controller plus the interface chips will sell for less than $50/set in volume lots. Samples are immediately available for the 91C100, and will be available in the fall for the PHY100.

***Standard Microsystems Corp.**, 80 Arkay Dr., Hauppauge, NY 11788; Doug Finke, (516) 435-6000.* **CIRCLE 800**

■ *DAVE BURSKY*

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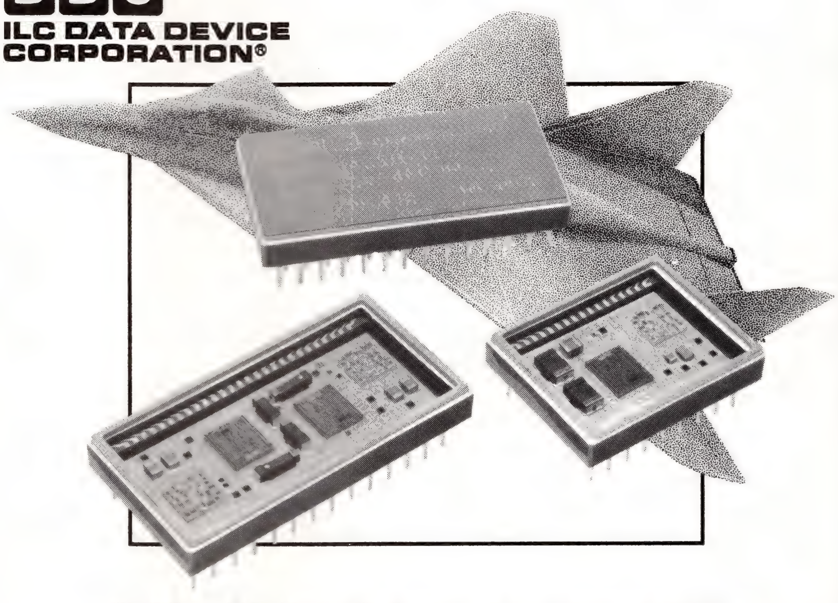

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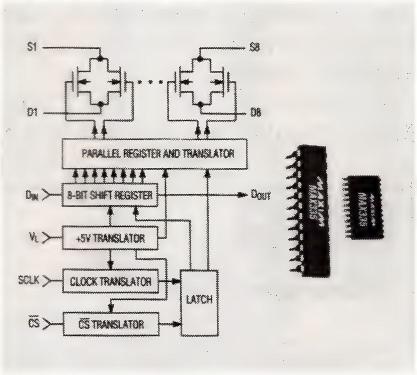
SPST SERIAL-CONTROLLED ANALOG SWITCHES COME IN 24-PIN PACKAGE

The 8-channel, single-pole single-throw (SPST) switch MAX335 can handle ±15-V analog signals. By equipping it with a three-wire serial digital interface, designers were able to cram it into a 24-pin package—both DIP and SOIC. Compatible with Motorola's SPI standard, the interface permits the switch to operate as a slave device.

The IC is operated by pulling the $\overline{CS}$ pin low and clocking the SCLK pin. Input control words on the D_{IN} pin are latched into internal shift registers on the rising clock edge. After shifting in 8-bits, the $\overline{CS}$ is pulled high, which transfers data from the serial register to the parallel register to directly update the switch. When V_L is below 2.4 V, all switches are set to the off state and the registers to all zeros, which guarantees all switches are off at power up. The D_{OUT} pin makes it possible for multiple MAX335s to be daisy chained.



Except for the serial interface, the IC is functionally equivalent to a pair of standard DG211 quad switches. Available for the commercial, industrial, and military temperature ranges, pricing starts at $2.84 each in lots of 1000.

***Maxim Integrated Products,** 120 San Gabriel Dr., Sunnyvale, CA 94086; Tony Vaccarella, (408) 737-7600, ext. 6087.*

CIRCLE 801

■ *FRANK GOODENOUGH*

LOW-POWER/LOW-VOLTAGE OP AMPS AVAILABLE IN TSSOP PACKAGE

A pair of dual high-performance CMOS operational amplifier are available in Thin Shrink Small Outline Packages. The TSSOP only requires half of the board area of a standard 8-pin small-outline-IC package.

Dubbed the TLC2262 and TLV2262, the former op amp operates with supply rails between 4.4 V and 16 V (±2.2 to ±4). Its data-sheet specifications are given with 5-V and ±5-V rails.

The TLV2262 operational amplifier is optimized for operation from a single 3-V supply rail. In addition, it can run with 2.7-V to ±8-V between the supply pins. Data-sheet specifications are given for 3-V and 5-V supplies.

Both the TLC2262 and TLV2262 op amps sport maximum quiescent currents of just 500 μA, while offering rail-to-rail output swing. Open-loop gain driving 50 kΩ runs a minimum of 98 dB.

Aimed at precision applications, the maximum offset voltage of the premium A-grade models runs just 950 μV, and no more than 1500 μV over the op amp's extended-industrial temperature range.

Bias current typically runs under 0.5 pA at 25°C, and a maximum of 500 pA over the temperature range. As with most low-power devices, ac performance suffers—but it is sufficient for dc, sub-audio, and voice applications.

In quantities of 1000 units, pricing for the operational amplifier in 8-pin dual in-line packages starts at just $0.82 each.

***Texas Instruments Incorporated,** Literature Response Center, Post Office Box 172228, Denver, CO 80217; (800) 477-8924, extension 4500.* CIRCLE 802

■ *FRANK GOODENOUGH*

12-BIT ADC SAMPLES AT 40 kHz

When the venerable 574 12-bit ADC IC was announced over 15 years ago, noone expected a sampling ADC with similar throughput rates that needed just 1 mA of current from a 3.3-V supply rail, or just 3.3 mW of power. But it has arrived in a tiny, 24-lead SOIC package. Called the HI5813, the ADC uses CMOS switched-capacitor technology.

The HI5813 is aimed at very low-power applications, ranging from cordless phones, DSP-based hearing aids, and portable medical and test instruments to PCMCIA Type II based data acquisition pc boards and pen-based PCs. It will also find homes monitoring critical voltages in a variety of systems. Because the HI5853 employs a switched-capacitor successive-approximation architecture, signal sampling is inherent. Its 25/35-μs minimum conversion time (J/k-grade) includes the time to acquire the signal.

While aperture uncertainty time is not specified, ac (dynamic) specifications are provided, albeit typical and not near Nyquist. Sampling a 1-kHz input signal at 500 kHz results in a signal-to-noise + distortion (SINAD) ratio of 63.9 dB for the J grade device. The K-grade achieves a SINAD of 61.5 dB sampling 1 kHz at 600 kHz. Sampling similar signals at the same frequencies results in a total harmonic distortion (THD) of –71 dB for the K grade, 2 dB less for the J grade.

End-point integral and differential linearity errors over the extended industrial temperature range (–40°C to +85°C) run a maximum of ±4 LSB for the J-grade and ±2.5 LSB for the K-grade. The HI5813 is available in 24-pin plastic DIPs and SOICs and ceramic DIPs. In quantities of 100, the J-grade plastic DIPs go for $9.50 each, while the K-grade run just 95 cents more.

***Harris Semiconductor Corp.,** P. O. Box 883, Melbourne, FL 32901; (800) 4-Harris, ext., 7199.* CIRCLE 803

■ *FRANK GOODENOUGH*

TRIPLE 8-BIT DACs REPLACE TRIMPOTS—ONLY 65¢/DAC†

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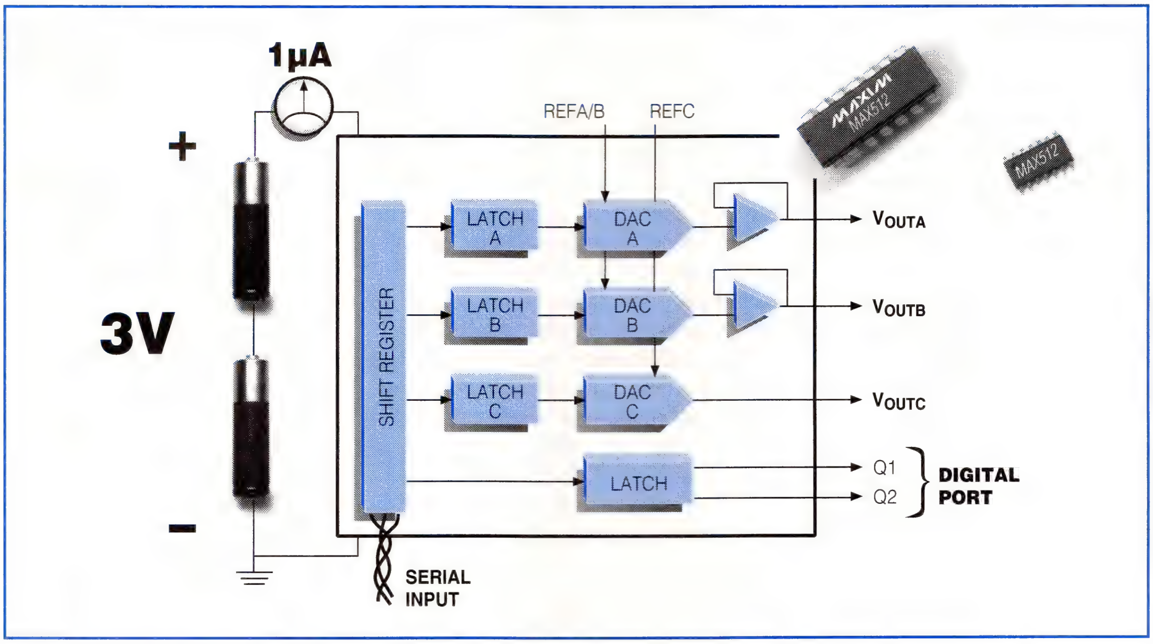

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MAX512 10,000 pc. price is $1.95, FOB USA

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READER SERVICE 97

64-BIT 68060 PROCESSOR DELIVERS 90 MIPS AT 50 MHZ

DAVE BURSKY

Maintaining software compatibility with previous-generation 680X0 family processors, the 68060 generation delivers close to double the performance of the 68040-class processors. Containing about 2.5 million transistors, the 68060 employs a deep pipeline and a dual-issue superscalar architecture, with branch cache and a high-performance floating-point unit, as well as dual 8-kbyte caches. With all the on-chip parallelism, the combination of integer, logical, and floating-point operations adds up to a total throughput of 250 million operations per second when running at 50 MHz—approximately equal to 90 VAX MIPS, and over 100 MIPS when clocked at 66 MHz.

In addition to the full-featured 68060 processor, Motorola also developed two reduced-cost versions—the 68LC060 and the 68EC060. The LC version lacks the floating-point capability of the 68060, so designers can trim system costs and power if high-speed floating-point computations aren't needed. For embedded application that also don't need the on-chip memory management logic, the 68EC060 offers the lowest cost/lowest power option.

Unlike Intel's Pentium processor, which employs a 64-bit data bus, designers at Motorola decided to use a 32-bit data bus so that existing 68040-based systems can be upgraded with a minimum of hardware redesign. Although the internal architecture of the 68060 is considerably different from the previous 68k family chips, externally the processor responds identically to 68040 instructions. To do that, the chips employ a dual integer pipeline that allows two instructions to start executing simultaneously.

The full Harvard architecture implemented in the data paths allows simultaneous access to both the data and instruction caches, and simultaneous operand read and writes. The separate 8-kbyte instruction and data caches can be frozen to prevent allocation over time-critical code or data. Instruction data-stream fetches, data-stream fetches, and external accesses can all occur simultaneously with instruction execution. The operand data cache employs a four-way banked architecture to permit simultaneous read and write accesses during each clock cycle.

A four-stage instruction-fetch pipeline decoded the variable-length instructions and turns them into fixed-length representation and channels them into an instruction buffer. The buffer acts as a FIFO register that helps to decouple the instruction-fetch unit and operand execution unit. The fixed-format instructions are then dispatched to dual four-stage pipelined RISC operand execution engines. Adding to the performance, the branch cache allows most branches to be executed in zero cycles by using a technique known as branch folding. The cache allows the instruction-fetch pipeline to detect and change the instruction prefetch stream before the change of flow affects the instruction execution engines, minimizing the need for pipeline refills.

Power management capabilities were added in addition to the use of fully static CMOS logic, which minimizes standby power drain. Dynamic power management minimizes power by allowing only the active stage of the pipeline to draw power when an access is being performed. A low-power stop instruction is also available to shut down the active circuits in the processor, thus halting instruction execution and placing the CPU into a standby mode. The 68060, though, operates from a 3.3-V supply but can interface to both 3-V and 5-V peripherals and logic.

Development support tools for the 68060 are available from over a dozen companies. Some of the suppliers include Diab Data, Eyring Corp., General Micro Systems, Hewlett-Packard, Huntsville Microsystems, Integrated Systems, Interconnect Systems, Intermetrics Microsystems Software, JMI Software Systems, Microtec Research/Ready Systems, Microware, Performance Computer, Software Developmen Systems, and Wind River Systems.

The 50-MHz versions of the 68060 LC060, and EC060 are now being sampled; 66-MHz versions are expected in third quarter of this year In lots of 10,000 units, the 50-MHz 68060 sells for $263, while the LC06 sells for $169 and the EC060 goes fo $150.

Motorola Inc., 6501 William Cannon Dr. West, Austin, TX 78735-8598; Tom Spohreer, (512) 891-2917. **CIRCLE 804**

■ *DAVE BURSKY*

GATE ARRAYS OFFER UP TO 667 KGATES

Offering eight masterslices with complexities from 52k to 667k total gates, and I/O counts ranging from 196 to 672 buffers, the HG72G/E family of gate arrays is optimized for operation from a 3-V supply. Fabricated with a 0.5-µm CMOS process, the logic dissipates a low 1.2 µW/gate/MHz—offering a better than seven-fold reduction in power, as opposed to the already available 5-V 0.8-µm family. On chip phase-locked loops, low-delay I/O buffers, low-skew clock trees, and high-speed static RAMs are all part of the design resources available to the engineer.

PLLs allow 100+ -MHz clocks with a 50% duty cycle, with only 500 ps of jitter, to be synthesized from external clocks; Gunning transceiver logic I/O buffers allow I/O transfers to operate at clock rates of over 100 MHz. Optional diffused memory blocks, with access times of as little as 3.5 ns and capacities of over 1 Mbit, can be added.

Metallized memory blocks of up to 256 kbits are also possible. The arrays will be available in high-lead-density ball-grid array packages, as well as ceramic pin-grid arrays with pin counts as high as 600 leads. NRE charges start at about $70,000, and sample delivery is three to four weeks after approved layout submission. DB

Hitachi America Ltd., Semiconductor and IC Div., 2000 Sierra Point Parkway, MS-080, Brisbane, CA 95005-1819; Jim Smith, (415) 244-7267. **CIRCLE 805**

WORLD'S SMALLEST MOST ACCURATE QUAD 12-BIT VOUT DAC

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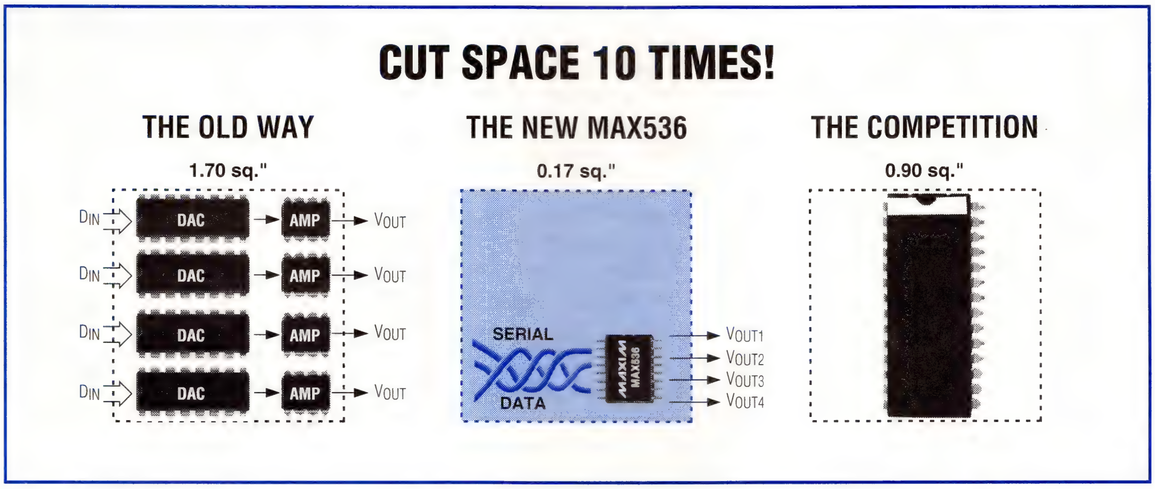
The MAX536/MAX537 is ideal for servo-control, offset/gain-adjust, and other applications where high precision and small form-factor are critical. 12-bit montonicity, ±1/2LSB relative accuracy, and ±1LSB Total Unadjusted Error* (MAX536) are guaranteed with no zero- or full-scale adjustments. The four DACs can be updated either independently or simultaneously via a single command register, and the serial interface is fully compatible with SPI™. QSPI™, and MicroWire™.



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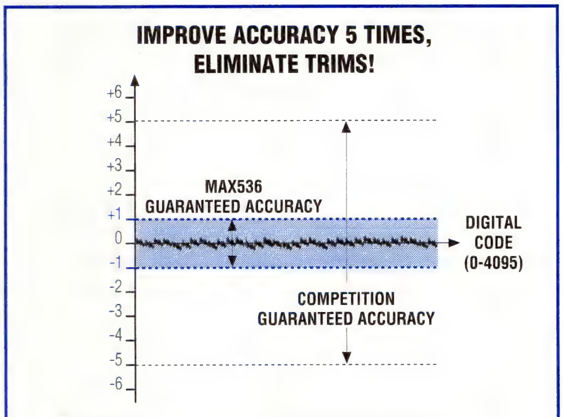

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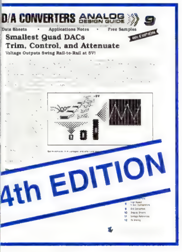

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Total Unadjusted Error (TUE) = Sum of Linearity, Offset and Gain Errors.

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READER SERVICE 100

DUAL-PROCESSOR CONTROLLER TACKLES PAGE PRINTERS

Containing more printer-specific support logic than any previously released microcontroller, the 68322 was developed jointly by Motorola and Peerless Systems Corp. to create a new price/performance point for page printers. Based on a 68000-family core processor, the 68322 also includes a raster engine that allows the processor to form the heart of 8-page/min. (or less) laser printers with resolutions of 600 DPI or less. The functions included in the controller suit the chip for mid- to low-end PCL/PostScript printers, as well as multifunction peripherals, inkjet printers, and other embedded applications.

On the chip are two distinct processors—a 68EC000 core microprocessor and a RISC graphics engine. The 68EC000 core performs the general-purpose computing, I/O handling, exception handling, and rendering of display lists. The RISC graphics engine includes two sections: one interprets the display lists and produces banded images; the other interfaces to the print engine, performing high-speed bit-block transfers (up to eight-times faster than most other printer controllers). The internal bus architecture and dual processing units allow the chip to perform parallel processing in addition to controlling DRAMs, peripherals, PROMs, font cartridges, and other functions.

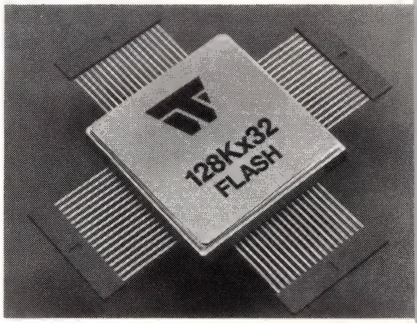
Available in 16- and 20-MHz speed grades, the 68322 can execute page-printer operations using banding algorithms. Banding schemes allow laser printers to minimize the need for DRAM by generating the image in real time in strips (referred to as bands), reusing a moderate amount of RAM rather than requiring 4 or more megabytes to store a full-page image. The chip processes a compressed display list to form the bit-mapped image of the page to be printed. The graphics engine on the chip also employs a high-performance DMA controller to quickly feed image data to the processor.

Additional resources on the processor chip include the system-integration module, which includes 8 programmable chip selects, an address space of 256 kbytes to 512 Mbytes, independently programmable timing for each bank of off-chip memory, interface support for font cartridges, and an integrated system timer. The DRAM controller can control up to six banks of DRAM and can address up to 48 Mbytes using standard addressing or burst transfer schemes. A full parallel port, compatible with the IEEE 1284 standard, is also included on the controller chip. Using the 68322, a minimum printer control subsystem would consist of the 68322, a clock, some reset logic, an optional memory, and communication devices.

In lots of 10,000 units, the 16-MHz version of the controller sells for $17.95 each, if housed in a 160-lead PQFP. Samples of all speed grades will be available this month.

Motorola Inc., 6501 William Cannon Dr. West, Austin, TX 78735-8598; Mike Frawley, (512) 891-2154. **CIRCLE 806**

■ *DAVE BURSKY*



FLASH MODULE READS, WRITES WITH 5-V

Organized as 128-kwords by 32-bits, the WF-128Kx32 flash-memory-based module employs a sectored architecture and requires just a 5-V supply for reads or writes from/to the nonvolatile storage cells. The 4-Mbit memory is divided into eight sectors of 16 kwords each, permitting updates to take place a sector at a time and potentially prolonging the life of the storage cells. Versions of the memory module are available with access times of 60, 90, or 120 ns, and all can endure a minimum of 100,000 erase/write cycles. The memory array has a typical standby current of just 1 mA and consumes less than 500 mW when active.

Housed in a 68-lead hermetic, ceramic quad-sided flat package that measures just 1.38-in. square and 0.215-in. high, (35-mm square and 5.5-mm high), the memory is qualified for operation over the industrial, -40 to +85°C range, or over the full military temperature range of -55 to +125°C. A low-profile package, just 0.14-in. high, is in development. Screening to military standard can meet the requirements of MIL-H-38534, and MIL-STD-883. The company is also certified to MIL-STD-1772. In lots of 100 units, prices for the military-temperature-range versions start at $500 each. Delivery is stock to eight weeks. DB

White Technology Inc., 4246 E. Wood St., Phoenix, AZ 85040; Jack Bogdanski, (610) 437-9120.

CIRCLE 807

32-BIT RISC CPU COMES AS STANDARD CELL BLOCK

Available with clock speeds as high as 40 MHz, the ARM6 RISC processor can be had as a standalone CPU or as a building block in the company's functional system block cell library. At 40 MHz, the 32-bit CPU delivers a peak throughput of 40 MIPS, but will typically sustain a throughput of about 26 MIPS when operated with a 5-V supply. There are three versions of the building block cell—the VYF86C06-001, -002, and -003, with each also available as models in Verilog and VHDL languages to ease simulation. The -001 version is similar to the standalone VY86C06040 CPU and is implemented with a 5-V, 0.6-μm process well suited for cost-sensitive consumer applications. A triple-level-metal process is used for the -002, thus suiting this version for high-density ASIC designs. Samples of the VY86C06040 come in 100-lead TQFPs. In lots of 100, it costs $27.00 each. DB

VLSI Technology Inc., 1109 McKay Dr., San Jose, CA 95131; Tom Schild, (602) 752-6373. **CIRCLE 808**

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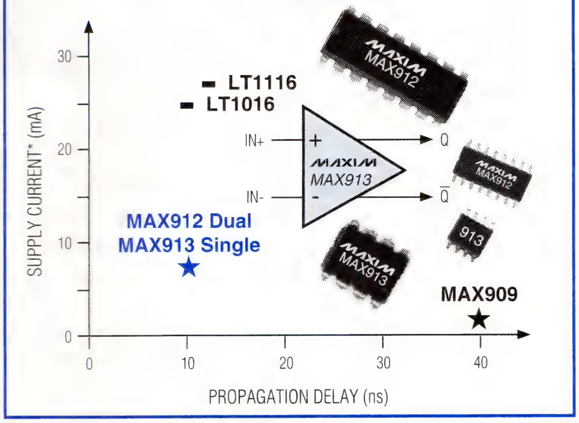

Select the Lowest-Power, High-Speed Comparators for Your Design

		COMPARATORS PER PKG	PROP DELAY (ns)	SUPPLY CURRENT* (mA)	INPUT VOLTAGE RANGE (V+ = 5V, V- = GND)	COMPLEMENTARY OUTPUTS
NEW	**MAX912**	**Dual**	**10**	**7**	**GND to 3.5V**	**YES**
NEW	**MAX913**	**Single**				
NEW	LT1016	Single	10	25	1.25V to 3.5V	YES
NEW	LT1116	Single	12	27	GND to 2.5V	YES
	MAX901	Quad	8	2.5	GND to 2.75V	NO
	MAX902	Dual				
	MAX903	Single				
	MAX907	Dual	40	0.7	GND to 3.5V	NO
	MAX908	Quad				
	MAX909	Single	40	1.2	GND to 3.5V	YES

*Positive Supply Current per Comparator; V+ = 5V, V- = GND.

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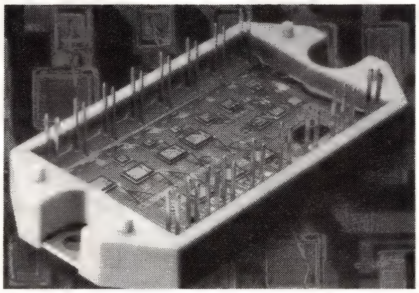
READER SERVICE 99

HYBRID IGBT POWER MODULE INTEGRATES MOTOR-DRIVE FUNCTION



Smarter, more energy-efficient control of variable-speed motors, power-conversion systems, and electric vehicles is made possible by a family of highly integrated hybrid power modules. Motorola's family of integrated power stages combine a three-phase input rectifier bridge, a three-phase output inverter, a brake transistor/diode, a current-sense resistor, and temperature sensor in one package.

The first in the family is the model MHPM7A15A60A, a 15-A, 600-V module housing seven IGBTs for the output inverter. Those transistors are matched with soft free-wheeling diodes to provide optimal dynamic performance. Other design features include access to both the positive and negative dc buses and a single-phase ac-input option.

Claimed as an industry first, the module's integration of an optional current-sense resistor and temperature sensor provides motor-efficiency feedback to the user's control board. The module's top connector pins are designed for an easy interface to that board. For evaluation and quick design-ins, Motorola is offering a gate-drive and protection board that's compatible with the module.

Configured as an integrated power stage for a minimum of 750 W (1 hp and below) motor drives, the module has applications in motor controls (factory automation, white goods, and industrial), servo controls, power conversion, office equipment, and electric vehicles. The MHPM7A15A60A module is the first of a family that will range from 15 to 30 A at 600 V and 5 to 15 A at 1200 V.

Pricing for the 15-A, 600-V module ranges from $45 to 50 in small lots to $30 to $35 in OEM quantities. Samples are available now with production quantities shipping in June with a two-to-four-week lead time.

***Motorola Semiconductor Products Sector**, 5005 E. McDowell Rd., Phoenix, AZ 85062-2953; Bill Roman, (602) 244-3103.* **CIRCLE 809**

■ *DAVID MALINIAK*

DUAL-OUTPUT SUPPLY MEETS BENCH NEEDS

Two zero-to-25-V dc outputs—enough to satisfy most bench requirements—are provided by the HP E3620A bench-top power supply. HP specifies both normal-mode voltage noise and common-mode current noise for the unit. The supply's 0.01% load and line regulation keep the outputs steady with changes in the power line and load. Separate digital panel meters monitor the voltage and current of either output simultaneously. All outputs are protected against overload and short-circuit damage. Pricing in single quantities is $500. Availability is scheduled for May. DM

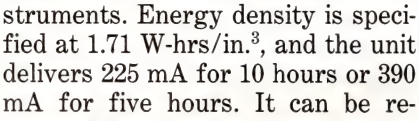
Hewlett-Packard Co., Direct Marketing Organization, P.O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844, ext. 8185. **CIRCLE 810**

LINEAR POWER SUPPLY ACHIEVES UL 544 RANK

UL 544 recognition has been achieved by the model 7010 linear power supply. The unit provides a low-noise, dual ±15-V dc output rated at 6 W. It's well suited for medical and dental applications where isolation is critical. Voltage accuracy is ±0.5% and line and load regulation are specified at ±0.04%. Noise and ripple are 1 mV rms. The supply's short-circuit protection features foldback current limiting, so all units can be shorted indefinitely without damage. The 3.5-by-2.5-by-1.25-in. case is fully encapsulated and overall weight is 17.5 ozs. Pricing is $111.90 in lots of 100. Delivery is from stock. DM

Calex Mfg. Co. Inc., 2401 Stanwell Dr., Concord, MA 94520; (800) 542-3355. **CIRCLE 811**

12-V RECHARGEABLES POWER PORTABLES



Pressure-contact terminals that fit typical video-tape recorders and portable cellular phones are featured in the model PS-1223 12-V, 2.3-Ah rechargeable sealed lead-acid battery. The battery's low-profile design, coupled with its high energy density, make it a versatile power source for systems such as portable PCs and instruments. Energy density is specified at 1.71 W-hrs/in.^{3}, and the unit delivers 225 mA for 10 hours or 390 mA for five hours. It can be recharged from 200 to 500 times, depending on the average depth of discharge. The package measures 7.17 by 0.94 by 2.42 in. and weighs 1.76 lbs. Pricing is $24.75 in 100s. DM

Power-Sonic Corp., P.O. Box 5242, Redwood City, CA 94063; (415) 364-5001. **CIRCLE 812**

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Low Voltage Comparators Plus 1.2V ±2% Reference Draw Less Than 6.5µA

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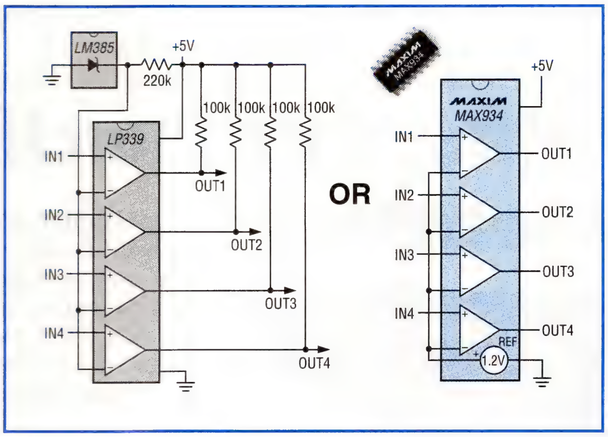
- **Programmable Hysteresis**
  - * No Effect on High-Z Inputs
  - * Independent of Supply Voltage
- **TTL/CMOS Outputs Source 40mA**
  - * No Pull-ups Required

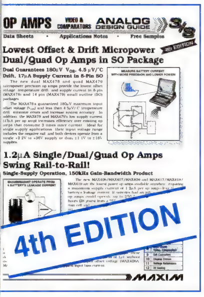


MAX934 low-cost quad comparator + reference single IC solution: 30-times LESS power, less board space, easier to use!

Ideal for 3V and 5V battery-powered applications, the new MAX931, MAX932, MAX933, and MAX934 are the lowest power single, dual, and quad comparators available. These devices include a 1.2V ±2% reference, programmable hysteresis (MAX931/MAX932/MAX933), and TTL/CMOS outputs that source over 40mA and eliminate external pull-up resistors. The quad MAX934 replaces power-hungry, two-chip alternatives, such as the industry standard LP339 and LM385 reference, resulting in a greater than 30-times reduction in power.

Choose the Lowest Power Comparators for Battery-Powered Systems

DEVICE		TOTAL SUPPLY CURRENT (µA Max, 25°C)	INTERNAL REF ACCURACY OVER TEMP	PROGRAMMABLE HYSTERESIS	PACKAGE
MAX931	Single + Reference	3.2	±2%	YES	8-DIP/SO
MAX932	Dual + Reference	4.5	±2%	YES	8-DIP/SO
MAX933	Dual + Reference	4.5	±2%	YES	8-DIP/SO
MAX934	Quad + Reference	6.5	±2%	NO	16-DIP/SO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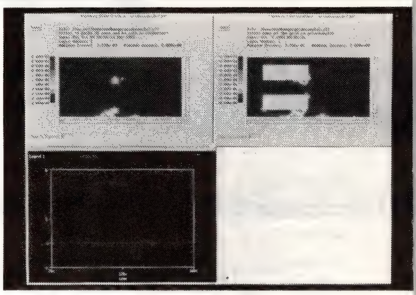
READER SERVICE 98

TOOLS HELP ANALYZE SIGNAL INTEGRITY

Two new products added to Ansoft's Maxwell family of signal-integrity tools help perform high-speed design analysis. The first product, SI Eminence, combines all the capabilities of the company's SI Spicelink product with a full-wave solver that examines high-speed and radiation effects. SI Spicelink is the company's existing extraction and simulation environment that's mainly used during the portion of the design cycle when full-wave and radiative effects may be ignored. The SI Eminence package offers tools for signal-integrity, electromagnetic-interference, and electromagnetic-compatibility analysis. SI Extractor, the second of the two products, performs both 3D RLC extraction and 2D RLGC extraction. The extracted parameters can be exported in Spice models so that users can simulate with Spicelink. Maxwell SI Eminence and SI Extractor are available now for Unix workstations. Pricing is set at $49,900 and $19,900, respectively. Maxwell SI Spicelink, which also runs on Unix workstations, costs $34,900. LM

Ansoft Corp., Four Station Square, Suite 660, Pittsburgh, PA 15219; (412) 261-3200. **CIRCLE 813**



PLD DESIGN SOFTWARE ADDS VHDL SUPPORT

Version 3.2 of the PLDesigner-XL software from MINC adds support for VHDL-based design entry. PLDesigner-XL is part of the company's family of synthesis tools for programmable logic, including FPGAs, complex PLDs, and simple PLDs. The 3.2 version adds support for a host of new devices, including Intel FLEXlogic, Lattice pLSI and ispLSI, and AMD Mach 445 and 465 parts. PLDesigner-XL speeds the design process with its patented automatic device fitting and multiple-device partitioning. In addition, it provides a consistent design environment for over 5,200 devices from a variety of manufacturers. The software runs on PCs, and on HP and Sun workstations. Engineers can choose from eight device-design modules, automatic partitioning, VHDL design entry, and a library interface to Synopsys tools. Pricing depends on platform and options. The personal-computer and Unix versions of the software start at $2995 and $4595, respectively. LM

MINC, 6755 Earl Dr., Colorado Springs, CO 80918; (800) 755-3742 or (71(0 590-1155. **CIRCLE 814**

Synthesized Function Generators

Direct Digital Synthesis is a powerful new concept for function generators, delivering synthesized accuracy and resolution, clean output waveforms and seamless frequency sweeps.

These three high performance instruments use DDS technology to provide a range of features, such as standard waveforms (sine, square, triangle ramp), built-in modulation, and arbitrary waveforms, making them suitable for a variety of benchtop and ATE applications.

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Frequency Resolution	1 µHz	1 µHz	1 µHz
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Maximum Output	20 Vpp (Hi Z)	20 Vpp (Hi Z)	20 Vpp (Hi Z)
THD (f_O=10 kHz)	< 0.05%	< 0.05%	< 0.10%
Spurs (f_O=1 MHz)	< -65 dBc	< -65 dBc	< -55 dBc
Modulation	FSK	FSK	AM, FM, PM, Burst
Arbitrary Waveforms	none	16K points	16K points
GPIB/RS232	$395	$495	$495
Price (U.S. List)	**$995**	**$1595**	**$2195**

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NEW PRODUCTS
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PLD TOOLS OFFER BROAD DEVICE SUPPORT

Version 2.00 of PLD Tools 386+ from OrCAD is a device-independent design environment that supports a broad range of programmable logic, including PLDs, complex PLDs, and FPGAs. Also, this latest PLD 386+ edition is integrated with both the company's SDT schematic tools and its VST verification and simulation software to provide a complete design environment. Users can describe their logic with either schematics or OrCAD's hardware design language (OHDL), or they can mix the two. They check their design's timing with the VST software, and then choose the programmable device that best fits their needs. Version 2.00 lets users design large, complex structures like wide adders and comparators, and then synthesize these quickly and efficiently. PLD 386+ 2.00, which is available now, runs on PCs. The $1895 price tag includes all device fitters, one year of technical support, access to the OrCAD bulletin board, and the company's newsletter. LM

OrCAD, 9300 S.W. Nimbus Ave., Beaverton, OR 97005; (503) 671-9500. **CIRCLE 815**

MODELS ARE AVAILABLE FOR PENTIUM FAMILY

Logic Modeling now has models available for the Pentium processor family. Two types of models are available: a full-functional hardware model and a bus-functional behavioral model. Hardware models for the Pentium 735/90 and Pentium 815/100 use the actual device in simulation. As a result, they represent all device functions, including undocumented behavior. The software behavioral model is a bus-functional model that incorporates all the bus cycles of the device, but uses a specialized language to control the model rather than the processor's standard instruction set. Both models are available now. The hardware model costs $8000, and works with the company's hardware-model servers. The software model is sold as a perpetual site license for $15,000. LM

Logic Modeling, 19500 N.W. Gibbs Dr., Beaverton OR 97006; (800) 344-0004. **CIRCLE 816**

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MODEL	CO-737	CO-738S
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READER SERVICE 128

ACQUISITION SYSTEM FITS THERMOCOUPLE TASKS

Users can connect up to 16 analog inputs to the built-in signal I/O panel of the DI-221TC, a portable battery-powered 12-bit data-acquisition system. Making the system particularly well-suited for thermocouple-based temperature measurement is a sensor attached to the termination receptacles to supply cold-junction compensation. Also, the DI-221TC linearizes thermocouple signals in real time with DSP-based 10th-order polynomial calculation software. This software works with other types of nonlinear transducers, as well. The unit plugs into the parallel port of any PC-compatible computer. The system accepts 0-5-V or 0-5-mV dc signals, or bipolar signals (±5 V or ±5 mV dc). The DI-221TC costs $1395 and is available from stock. JN

Dataq Instruments Inc., 150 Springside Dr., Ste. B220, Akron, OH 44333-2473; (800) 533-9006 **CIRCLE 817**

Z80 EMULATOR INCLUDES PERFORMANCE ANALYSIS

The UEM-Z80 supplies high-performance Windows-based in-circuit emulation for the Z80 microprocessor. The unit has a performance analyzer that monitors time spent in up to 255 routines simultaneously, with better than 100-ns accuracy. Included is a Windows-hosted source-level debugger for C and assembly language. The UEM-Z80 has 131,072 hardware breakpoints. Breakpoints can also be set on data values, and the unit supports complex breakpoints with conditions five levels deep. A 4-kbyte trace buffer generates views of the data as raw machine instructions, C source, or intermixed C and disassembled code. Triggers qualify trace data collection, limiting acquisition to events of interest. The UEM-Z80 costs $5500 and is available from stock. JN

Softaid Inc., 8310 Guilford Rd., Columbia, MD 21046; (800) 433-8812 or (410) 290-7760 **CIRCLE 818**

MEMORY TESTER HANDLES MULTIPLE DEVICES

The MTX is a massively parallel functional test system for memory devices. Available with hot or hot/cold environmental chambers, the MTX handles DRAMs, SRAMs, flash, and most application-specific memories. The system has up to 30 test board slots with 256 channels each. Also, each slot has up to eight reconfigurable electrical test zones and individual power supplies. Up to 12,000 devices can be tested in a hot chamber and up to 7200 in a hot/cold chamber. The unit features a 20-MHz algorithmic pattern generator. The MTX can also be used as a test-during-burn-in system to ensure the reliability and quality of burned-in devices. Optional fault analysis capability is available. MTX prices range from about $550,000 to $1 million, depending on configuration. JN

Aehr Test Systems, 1667 Plymouth St., Mountain View, CA 94043; (415) 691-9400 **CIRCLE 819**

ADVERTISEMENT

Small Company's New Golf Ball Flies Too Far; Could Obsolete Many Golf Courses

Pro Hits 400-Yard Tee Shots During Test Round

Want To Shoot An Eagle or Two ?

By Mike Hensen

MERIDEN, CT – A small golf company in Connecticut has created a new, super ball that flies like a U-2, putts with the steady roll of a cue ball and bites the green on approach shots like a dropped cat. But don't look for it on weekend TV. Long-hitting pros could make a joke out of some of golf's finest courses with it. One pro who tested the ball drove it 400 yards, reaching the green on all but the longest par-fours. Scientific tests by an independent lab using a hitting machine prove the ball out-distances major brands dramatically.

The ball's extraordinary distance comes partly from a revolutionary new dimple design that keeps the ball aloft longer. But there's also a secret change in the core that makes it rise faster off the clubhead. Another change reduces air drag. The result is a ball that gains altitude quickly, then sails like a glider. None of the changes is noticeable in the ball itself.

Despite this extraordinary performance the company has a problem. A spokesman put it this way: "In golf you need endorsements and TV publicity. This is what gets you in the pro shops and stores where 95% of all golf products are sold. Unless the pros use your ball on TV, you're virtually locked out of these outlets. TV advertising is too expensive to buy on your own, at least for us.

"Now, you've seen how far this ball can fly. Can you imagine a pro using it on TV and eagle-ing par-fours? He would turn the course into a par-three, and real men don't play par-three's. This new fly-power forces us to sell it without relying on pros or pro-shops. One way is to sell it direct from our plant. That way we can keep the name printed on the ball a secret that only a buyer would know. There's more to golf than tournaments, you know."

The company guarantees a golfer a prompt refund if the new ball doesn't cut five to ten strokes off his or her average score. Simply return the balls–new or used–to the address below. "No one else would dare do that," boasted the company's director.

If you would like an eagle or two, here's your best chance yet. Write your name and address and "Code Name S" (the ball's R&D name) on a piece of paper and send it along with a check (or your credit card number and expiration date) to National Golf Center (Dept. S-606), 500 S. Broad St., Meriden, CT 06450. Or phone 800-285-3900 anytime. No P.O. boxes. One dozen "S" balls cost $24.95, two to five dozen are only $22.00 each, six dozen are only $109.00. You save $40.70 ordering six. Shipping and handling is only $3.50 no matter how large your order. Specify white or Hi-Vision yellow.

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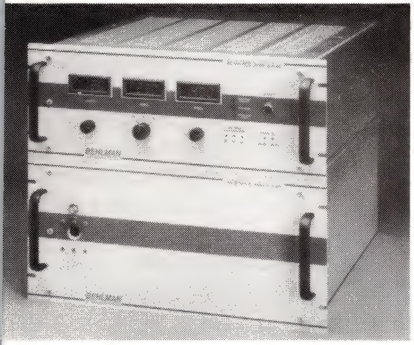
HIGH-POWER SOURCES ARE COMPACT, EFFICIENT

A pair precision single-phase ac power sources supply up to 12 KVA in as little as 15.75 in. of panel height in a standard rack mount. The BL6000 (6 KVA) and BL12000 (12 KVA) have IEEE-488 and RS-232 interfaces that allow remote control of frequency (45 to 500 Hz standard, 1000 Hz optional) and voltage (0 to 270 V split single phase). The unit features a digitally controlled waveform synthesis technique that produces the clean power of a linear supply with the small size and high efficiency of a switching supply. Protection circuitry creates voltage foldback during overloads to maintain undistorted waveforms. A multiphase input transformer offers low harmonic distortion and a high input power factor. The BL6000 costs $9995, and the BL12000 is $14,995. Delivery is from stock to 45 days. JN



Behlman Electronics, 6 Nevada Dr., Lake Success, NY 11042; (800) 645-8454 or (516) 328-1600 **CIRCLE 820**

PORTABLE OTDR BOASTS MODULAR FLEXIBILITY

The MW9070A is a handheld optical time-domain reflectometer with full benchtop features. The unit's modular design allows users to change optical modules in the field. Currently available are 1310-nm and 1310/1550-nm single-mode modules. Multimode modules are being developed. The MW9070A automatically measures splice and fault location with one button press. Optimal distance and pulse width are selected automatically. The battery-powered unit detects fiber faults, points of high reflection, far end points, and splice and connector losses down to 0.1 dB. It displays the waveform and event table simultaneously on a 7-in. variable-contrast LCD screen. Dynamic range is 23.5 dB, with a near-end dead zone of 10 m. The MW9070A prices range from $10,600 to $15,600. JN

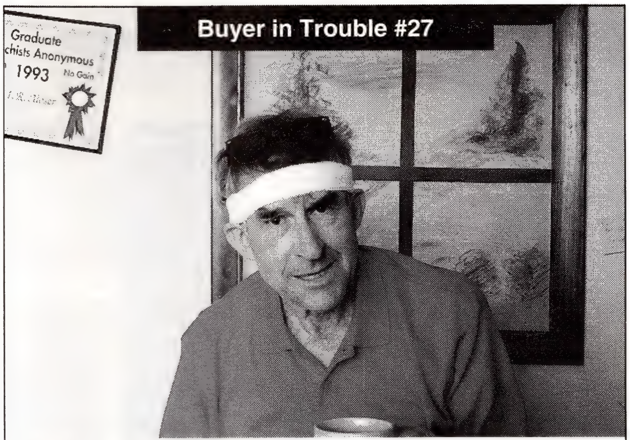
Anritsu Wiltron Sales Co., 685 Jarvis Dr., Morgan Hill, CA 95037-2809; (408) 776-8300 **CIRCLE 821**

68341 GETS TWO LEVELS OF EMULATION SUPPORT

Two levels of emulation support are available for Motorola's new 68341 microprocessor. The full-capability EMUL16/300-PC emulator board and the low-cost EMUL16/300-PC/BDM background debug mode emulator support the 3.3- and 5-V versions of the 68341 at its full-rated 25-MHz clock speed. The EMUL16/300-PC supports the 68341 through the POD-341 probe. The probe includes several sizes of emulation RAM, an oscillator, a serial connector, and 5-V power for the target. The EMUL16/330-PC/BDM is for users who do not need emulation memory, dynamic data exchange, instruction tracing, and shadow RAM support. This unit supplies source debugging and software breakpoints. Both units are available now directly from Nohau or through Motorola sales channels. Demonstration disks are available. The EMUL16/300-PC/BDM costs $995 alone, or $1495 with a high-level debugger. Prices for the EMUL16/300-PC start at $7290 and depend on trace size and other options. JN

Nohau Corp., 51 E. Campbell Ave., Campbell, CA 95008; (408) 866-4493 **CIRCLE 822**

Buyer in Trouble #27



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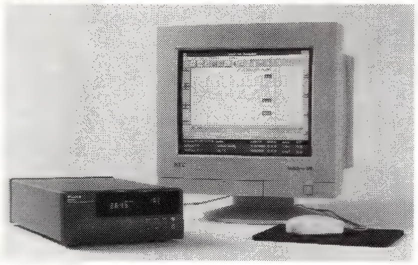
READER SERVICE 115

PC-BASED DATA SYSTEM CONNECTS TO ETHERNET



A pair of networked data-acquisition units supply portable 20-channel instruments that can be connected directly to a PC or to an Ethernet network. Also available for use with the NetDAQ instruments is a Windows-based software package with powerful trend-plotting capabilities.

The model 2640A takes measurements at 100 readings/s, with 5.5-digit resolution and 0.01% accuracy. The 2645A offers 1000 readings/s, 4.5-digit resolution, and 0.02% accuracy. The instruments include signal-conditioning circuitry. Included is the patented Universal Input Module, which allows users to directly connect a mix of inputs, such as thermocouples, ac and dc voltage, RTDs, resistance, current, and frequency. The module can be removed for easy reconfiguration. Eight digital I/O lines on the rear panel may be individually assigned, including use as alarm outputs.

Both units come in two versions, one with a standard chassis for an operating temperature range of 0 to 60°C, and one with an industrial chassis that allows wall and cabinet mounting and is rated for –20 to +70°C. Users without a network can connect the instruments directly to a PC through a network interface card or through a parallel port with a parallel-to-LAN adapter.

The software, called NetDAQ Logger for Windows, eliminates the need for custom programming or complex system integration. The Trend Plotting feature allows users to view and analyze current or historical data and to zoom in and out to view specific time spans or data. Users can print results or transfer files to other Windows applications. In the Grouped Mode, users can group channels from different NetDAQ units together for custom monitoring and analysis. The Spy Channe feature lets users monitor up to eight channels in real time. Finally the Computer Channel feature provides up to 10 additional channels to display statistics.

The 2645A and 2640A both cost $3995. The NetDAQ Logger for Windows software costs $1295 in a version for isolated networks, and $1995 for a shared-network version.

***Fluke Corp.**, P. O. Box 9090, Everett, WA 98206-9090; (800) 443-5853 or (206) 356-5500.* **CIRCLE 823**

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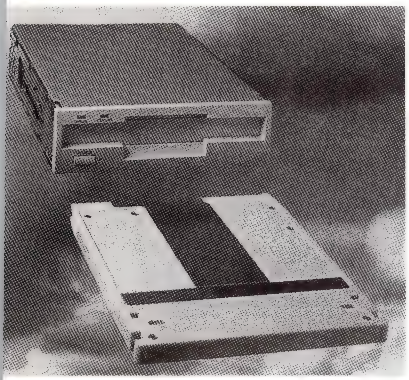
READER SERVICE 122

MO DRIVE FITS HALF-HEIGHT FORM FACTOR

With the ability to store up to 1.3 Gbytes, the JY-800 magneto-optical MO) disk drive fits a 5.25-in. half-



height form factor. The unique hologram laser pick-up allows the drive to be mounted in a vertical or horizontal fashion. Because the drive can handle over 10 million continuous read and write cycles, it can serve as a hard-disk drive replacement. The average seek time is 40 ms, while the effective transfer rate is 2 Mbytes/s. Available now, the JY-800 MO drive sells for $2400. A 650-Mbyte version, the JY-7000, is available for $1900. Prices are for quantities of 100. RN

Sharp Electronics Corp., Microelectronics Group, 5700 N.W. Pacific Rim Blvd., No. 20, Camas, WA 98607; (206) 834-2500. **CIRCLE 824**

HARD DISK DRIVES EXCEED 1 GBYTE

High-end desktop computers are the target of the latest hard-disk drives to enter the Caviar family. The AC31000 and AC2700 store 1.096 Gbytes and 730 Mbytes, respectively, each in a 3.5-in. form factor. The drives are built with an Enhanced IDE interface, which builds on standard IDE. Enhanced IDE adds high-speed host-transfer capabilities, support of high-capacity disks (above 528 Mbytes), and multiple device connectivity. As a result, non-disk-drive peripherals, such as a CD-ROM or tape drive, can be connected. The drives are designed with a caching architecture to increase the average transfer rate. Both drives are available now. RN

Western Digital Corp., 8105 Irvine Center Dr., Irvine, CA 92718; (714) 932-5000. **CIRCLE 825**

X-TERMINALS ADD TOUCH CAPABILITY

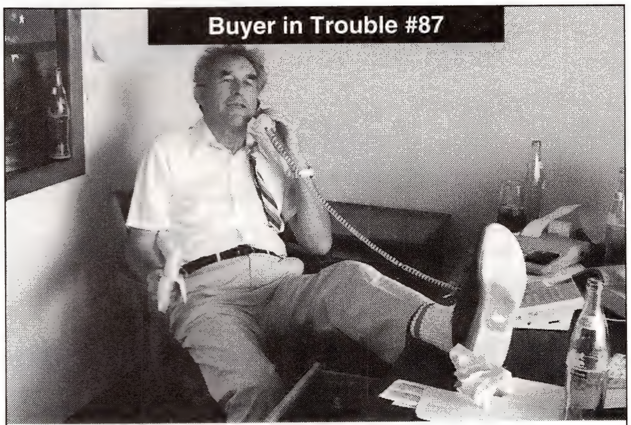
Touch-screen capability has been incorporated into the T series of monochrome and color X terminals. The displays range from 14 to 20 in. The touch screen employs a touch-sensitive glass panel and a Touch Interface Device (TID). When a user touches the screen, the TID maps the position of touch to a mouse-click action. Most standard operating environments are supported, including Solaris, VMS, AIX, HP/UX, and DG/UX. Five models are available. The 19TM is a 19-in. monochrome model that offers 1280- by 1024-pixel resolution. The 14TC1, 15TC1, and 17TC1 are 14-, 15-, and 17-in. color version, all with 1024- by 768-pixel resolution. The 20TC2 has a resolution of 1280 by 1024 pixels in a 20-in. monitor. Prices range from $3395 to $5195. RN

Phase X Systems Inc., 19545 N.W. Von Neumann Dr., Beaverton, OR 97006; (503) 531-2400. **CIRCLE 826**

SCSI DRIVE BOASTS 0.1-MS ACCESS TIME

An access time of 0.1 ms is the main feature of the Clipper solid-state storage device. Fitting a 5.25-in. full-height form factor, the drive employs DRAM to store up to 512 Mbytes. The drive emulates a SCSI-based hard-disk drive, so it requires no special drivers or other software. The Clipper integrates error detection and correction, an internal battery, and a two-level backup system. The drive is intended for data-intensive applications, such as scientific modeling, image processing, graphics manipulation, and transaction processing. The fast SCSI-2 port, available with either a single-ended or differential interface, supports 10-Mbyte/s data transfers. Prices range from $2615 for 16 Mbytes to $38,995 for a unit with 512 Mbytes. RN

Curtis Inc., 418 West County Rd. D, St. Paul, MN 55112; (612) 631-9512. **CIRCLE 827**


Buyer in Trouble #87

Plan It of the Apes

"Howard, my boss, said I was dumber than an orangutan for buying 400,000 transformers from offshore instead of calling Prem. He said Prem has no minimum order quantity and you can schedule deliveries when you need them. He threatened to let scientists dissect me to see if I'm the missing link.

I *really* shoulda called Prem.

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READER SERVICE 116

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DISK ARRAY OFFERS MODULARITY

Designed for the desktop, the Power Array family is a modular disk array that works with most standard environments, including Novell and Macintosh. Built around docking stations and shock-mounted removable modules, the array can store more than 8 Gbytes when fully configured. A duplexed fast SCSI 2 interface supplies a transfer rate of 20 Mbytes/s. Through software, RAID levels 0, 1, and 5 can be supported to ensure data integrity. Each docking station is available with one or two slots, and the drives can be hot-swapped. Surface-mount backplane technology improves the reliability. Prices start at $2899. RN

Mega Drive Systems Inc., 489 S. Robertson Blvd., Beverly Hills, CA 90211; (310) 247-0006. **CIRCLE 828**

PEN EMITS ELECTRONIC AND TRADITIONAL INK

The inking pen used on a digital-electronic environment now works in a traditional paper environment, as well. In addition, the pen needs no batteries. The pen drops both regular and electronic ink simultaneously, letting the user run parallel systems. The pen supplies visual feedback without expansive LCD technology. It operates with standard electromagnetic resonance, and is pressure sensitive, lightweight, and durable, providing a pen-and-paper feel. The inking pen is compatible with most of the pen-based platforms that are currently shipping. Available now, its price is under $50 in quantities of 10,000. Optional cartridges can also be purchased. RN

Wacom Technology Corp., 4633 Old Ironsides Dr., Suite 308, Santa Clara, CA 95054; (408) 982-2727. **CIRCLE 829**

SIMMS HOLD 32 MBYTES OF MEMORY

Two SIMM families each pack up to 32 Mbytes of memory with configurations as wide as 8 Mbits by 40 bits for the 72-pin models. The 30-pin DRAM modules are available in 8- and 9-bit data widths. The parts employ 16-Mbit DRAMs to achieve the high density in a 1-in.-high board. Using thinner-chip packages enables a single-sided thickness of 0.208 in. Access times are 60 ns. All versions operate in fast-page mode and offer three variations of refresh. Prices start at $1650. RN

Hitachi America Ltd, S & IC Div., 2000 Sierra Point Pkwy., MS-080, Brisbane, CA 94005-1819; (800) 285-1601, ext. 11. **CIRCLE 830**

PCMCIA DRIVE CONNECTS THROUGH SCSI INTERFACE

Any VMEbus or other platform that's equipped with a SCSI interface can connect to the MCDISK-E PCMCIA memory-card drive. The open-frame drive fits a 3.5-in. form factor and accepts all types of SRAM, flash EPROM, and OTP memory cards with capacities up to 64 Mbytes. The drive can handle cards that fit any standard form factor. The built-in 1-Mbyte/s SCSI interface supports the complete SCSI command set. Available now, the MCDISK-E costs $395. RN

Gespac Inc., 50 W. Hoover Ave., Mesa, AZ 85210; (602) 962-5559. **CIRCLE 831**

PCI AND VL-BUS DRIVE PCS

While the heart of the MicroFlex family of PCs is a Pentium microprocessor, the two latest models are driven by PCI and VL-Bus local buses. The base configuration for both systems includes 8 Mbytes of RAM, expandable to 128 Mbytes, a 500-Mbyte IDE hard-disk drive, 256 kbytes of cache memory, a 14-in. color display, DOS 6.2, and Windows 3.1. Video accelerators enhance graphics performance. The motherboards have room for eight slots—five 16-bit slots and three VL or PCI slots. Both systems cost $3250. RN

Micro Express, 1801 Carnegie Ave., Santa Ana, CA 92705; (714) 852-1400. **CIRCLE 832**

Accessories for rf testing

PCB emissions scanner • Locates low-to-high emissions, displays color image, stores data for design corrections at development stage.

Dual-directional couplers • Seven models up to 15 kW, matched to AR amplifiers and antennas.

Ultra-broadband E-field monitor • Four-channel capability, 1 to 300 V/m, isotropic probes cover 10 kHz to 1000 MHz or 80 MHz to 40 GHz.

Broadband fiberoptic data links • Modular plug-in analog systems for acquiring and measuring interference data, stimulating EUT, displaying results in color or monochrome, 10 kHz to 1 GHz.

Fiberoptic CCTV systems • Watch performance of EUT under hostile EMI and/or EMP shielded-room conditions, in color or monochrome.

TEM cells • Half again the bandwidth of comparable-size chambers: To 750 MHz for 15-cm EUT, 375 MHz for 30-cm EUT.

Computer bus interfaces • Two models, for isolated GPIB connection or isolated TTL connection, permit remote operation of amplifiers.

RF connection kit • Things you'd search for around the lab: Cables, coax adapters, connectors, fuses, lamps, fabricated cables.

Power combiner/dividers • Combine signals from four amplifiers, or divide one signal into four outputs.

High-power rf matching transformers • Match 50-ohm input to 12.5- or 200-ohm output. Up to 2 kW cw.

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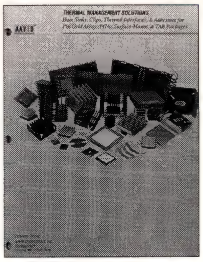
READER SERVICE 133

CATALOG/LITERATURE REVIEW

Heat sinks for microprocessors



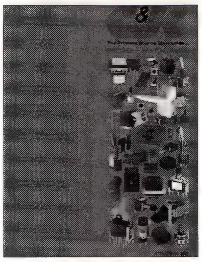
New 36-page catalog covers heat sinks, clips, double-sided tapes, adhesives, thermal interface materials, and fan heat sinks for cooling CPUs in PGA, surface mount and TAB packages. Contains CPU heat sink selector guide.

Call 603-528-3400.

CIRCLE 170

AAVID ENGINEERING, INC.

C&K's New Switch Catalog

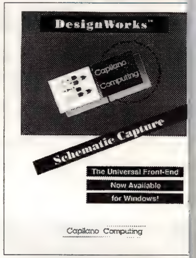


Offering the broadest line of switch products, C&K's new Catalog #9308 provides valuable design information for wide range of applications. Complete photo descriptions and specifications, along with electrical ratings, mechanical ratings, mechanical operation characteristics are included.

CIRCLE 171

C&K Components, Inc.

SCHEMATIC CAPTURE

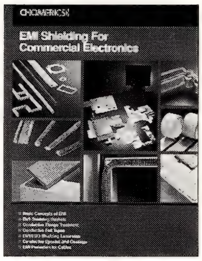


This brochure details Design Works for Windows, the universal front end for use with PCB, FPGA, Asic and spice packages. Software features full hierarchy, automatic gate packaging and 13,000 + symbols.

CIRCLE 172

Capilano Computing

COMMERCIAL EMI SHIELDING

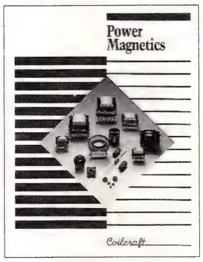


Chomerics EMI gasket products for meeting FCC and other commercial shielding requirements. Features basic EMI concepts, typical applications, gasket attachment systems and selection guide. Includes part nos and sales offices.

CIRCLE 173

Chomerics

Power magnetics featured

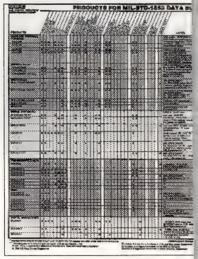


New 48-page catalog includes surface mount magnetics, switching power transformers, output filter chokes, current sensors, common mode line chokes, and variety of other devices. Also covered are Coilcraft's designer's kits that speed prototyping.

CIRCLE 174

Coilcraft

Data Bus Selection Chart

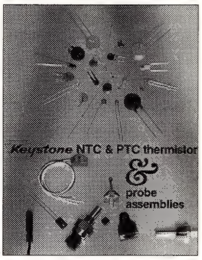


MIL-STD-1553 Data Bus selection chart lists over fifty products. It includes the latest in single & Dual Transceivers, Bit Processors, RTs, Interfaces, SEMs, Card Assemblies and test Equipment.

CIRCLE 175

ILC DATA DEVICE CORP.

NTC & PTC THERMISTORS

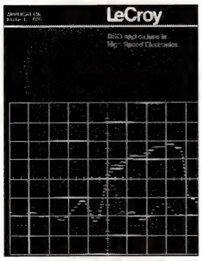


Covers thermistor engineering application for NTC & PTC & probes including inrush current, glass bead, surface mount, precision, cryogenic & hi-temp units plus resettable fuses, surface temperature sensors and heaters.

CIRCLE 176

Keystone Carbon Co.

DSO'S In High-Speed Electronics



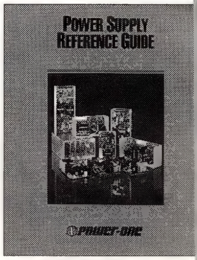
LeCroy offers a new application note for Design Engineers. Topics addressed include: measurements in noise, cross-channel timing crosstalk, microprocessor crashes, timing problems due to clock skew & more

Call 800-4 LeCroy.

CIRCLE 177

LeCroy

Power-one Power Supplies

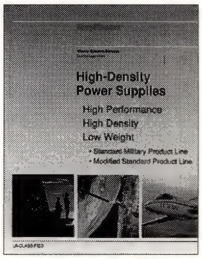


Power-One Reference Guide has over 200 switch-mode and Linear AC to DC Power supplies. Available direct or through distributors, model outputs range from 2V to 250V, up to 2000 watts, single and multiple outputs.

CIRCLE 178

Power-One, Inc.

High Density Power Supplies

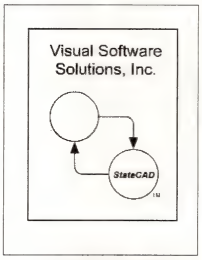

High-Density Power Supplies
High Performance
High Density
Low Weight
• Standard Military Product Line
• Modified Standard Product Line

A 6 page color brochure provides information on STND & Modified STND, High Performance E DC/DC converters for military & space applications. Brochure reviews converters designed for high efficient low noise, & pulsed power.

CIRCLE 179

Raytheon Quincy

State Machine Design

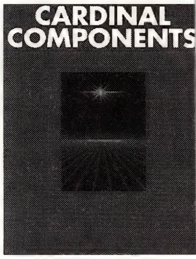


Material from Visual Software Solutions, Coral Springs, Flo, describes State CAD, a window 3.1 tool for state machine entry, analysis, automatic HDL generation, and documentation. Appnote, demo disk, and tutorial included.

CIRCLE 180

Visual Software

CRYSTALS AND OSCILLATORS

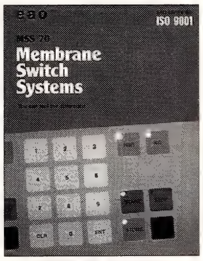


Cardinal Components Inc. , Montclair, N.J. has designed a user-friendly guide to Crystals and Oscillators. It features their complete line of components, including SMD and miniature packages.

CIRCLE 181

Cardinal Components Inc.

MEMBRANE SWITCHING SYSTEM

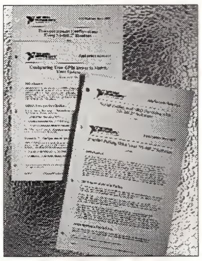


EAO Switch Corp., Released its New MSS 70 Catalog. Mounting Dimensions, Photos & Specs are included. MSS 70 Series offers unparalled flexibility as it is designed for custom membrane switching applications. ISO 9001!

CIRCLE 182

EAO Switch Corporation

GPIB Technical Notes

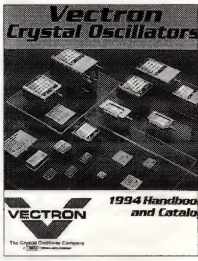


New technical notes on "GPIB Polling and SRQ Servicing" present tutorials on serial and parallel polling as well as how to use the industry-standard NI-488.2 software to perform polling tasks.

CIRCLE 183

National Instruments

CRYSTAL OSCILLATOR CATALOG



Vectron has published its new 1994 Crystal Oscillator Catalog. The comprehensive catalog details vectrons complete product line including clock and sinewave oscillators, TCXO'S, OCXO'S. VCXO'S and Sonet CDR products.

CIRCLE 184

Vectron Laboratories

Design Tools with Power

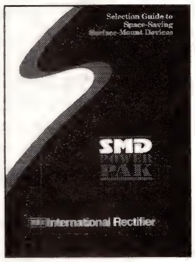
ango for DOS and goPro for Windows™: tronic design software C-based systems fea- g ease-of-use, per- ance & value.

CIRCLE 185

CCEL TECHNOLOGIES, INC.

Power SMDs Selection Guide

Some 250 space-saving surface mount devices covering both N and P channel power MOSFETS, Schottky diodes, IGBTs, and MOS Gate Drivers are all featured in this SMD Product Selection Guide from International Rectifier, El Segundo, CA.

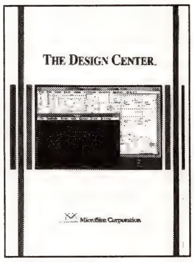


CIRCLE 186

INTERNATIONAL RECTIFIER

Design Center EDA System

With Microsim's Design Center, select from schematic entrys, circuit simulations prorammable logic synthesis, and signal integrity analysis to build a Custom integrated analog, digital, or mixed analog/digital desktop EDA system.



CIRCLE 187

MICROSIM CORPORATION

Power-one Power Supplies

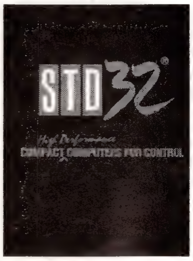
Power-one Reference Guide has over 200 switch-mode and linear AC to DC Power supplies, available direct or through distributors, model outputs range from 2V to 250V, up to 2000 watts, single and multiple outputs.

CIRCLE 188

POWER ONE, INC.

Small Industrial Computers

Brochure reviews STD 32, an 8-, 16-, and 32-bit industrial computer standard combining PC functionality and a compact format. A short form spec and list of manufacturers are included.

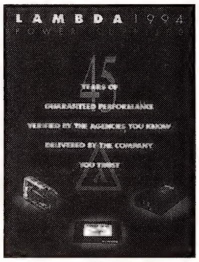


CIRCLE 189

SIG 32

POWER SUPPLIES

A new 168 page full line catalog is available on request from Lambda Electronics Inc., N.Y.. It contains detailed information and prices on over 1000 standard power supplies, systems and accessories including 200 new products.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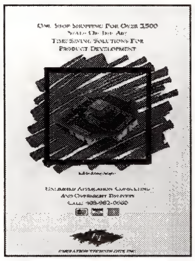
45 YEARS OF GUARANTEED PERFORMANCE
VERIFIED BY THE AGENCIES YOU KNOW
DELIVERED BY THE COMPANY
YOU TRUST

CIRCLE 190

LAMBDA ELECTRONICS INC.

VLSI/SMT SOLUTIONS CATALOG

Free '94 catalog. Over 00 devices; 120 "off-the- elf" items available for ernight delivery. Unlim- d application consulting. k about our custom de- gns. Leading edge tech- logy —over 500 PQFP lutions. Time Saving lutions.



CIRCLE 191

EMULATION TECHNOLOGY

C-Programmable Controllers

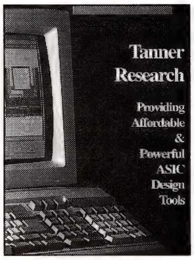
Save time and money. Our controllers are ideal for control, test or data acquisition applications with a mix of analog/digital I/O, relays, RS232/485 serial ports, LCD/keypads, & programmed with Dynamic C™. From $159, Qty. 1. (916) 757-3737, or Fax: (916) 753-5141. For 24 Hr. data, call from YOUR Fax: (916) 753-0618.

CIRCLE 192

Z-World Engineering

ASIC Design Software

Tanner Research, Pasadena, Calif., has a new brochure with detailed information on its complete line of affordable CAE/CAD software for ASIC design and layout. A free demo disk and price list are included.

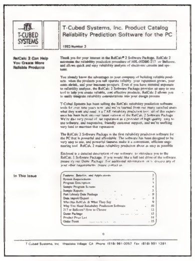


CIRCLE 193

TANNER RESEARCH

eliability Prediction

atalog describes the elCalc2 software ackage, which auto- ates Mil-HDBK-217 r Bellcore on your PC, nd allows quick and asy reliability analysis f your electronic prod- cts. Phone: (818) 91-0057 Fax: (818) 91-1281


T-CUBED SYSTEMS
T-Cubed Systems, Inc. Product Catalog
Reliability Prediction Software for the PC

CIRCLE 194

-Cubed Systems

PROTO EXPRESS

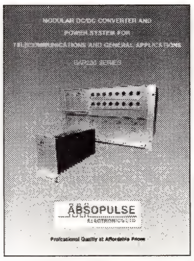
Multilayer prototypes in 1 to 5 days. FR4 and polyimide. Commerical or Milspect capabilities *buried/blind VIAS* carbon paste* up to 22 layers. Call Ken or Joycie 408-735-7137 phone 408-735-1408.

CIRCLE 195

Proto Express

Battery Chargers

The PFC Rectifier delivers 500W to load or Battery (2500W per rack), Features include full electronic protection, redundancy, high MTBF and hot swapping. The series is available in rack mount or stand-alone format.


MODULAR DC/DC CONVERTER AND POWER SYSTEM FOR TELECOMMUNICATIONS AND GENERAL APPLICATIONS
ABSOPULSE ELECTRONICS LTD
Professional Quality at Affordable Prices

CIRCLE 196

Absopulse Electronics

Highspeed Waveform Capture

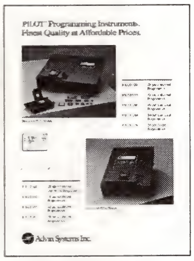
Signatec, Corona, CA. - binder containing data eets for all of its pc based roducts for use in the ar- as of waveform capture, aveform generation and gnal processing can be btained by contacting em at (909) 734-3001

CIRCLE 197

Signatec Inc.

DEVICE PROGRAMMERS

Affordable, dependable & versatile, Advin offers a full line of device programmers. All pkg types supported. IC mfrs approved. Free lifetime s/w updates via electronic BBS. Call for free catalog & latest supported devices list.

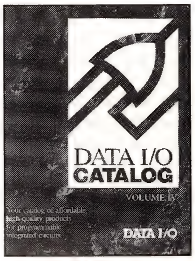

PILOT Programming Instruments.
Finest Quality at Affordable Prices.
Advin Systems Inc.

CIRCLE 198

Advin Systems Inc.

MADE TO ORDER

The Data I/O catalog makes our affordable tools easy to order. Phone, Fax, or mail in your order, and we'll deliver great values on high-quality design software and device Programmers. Call today for your FREE catalog.



CIRCLE 199

DATA I/O CORPORATION

MAJOR LEAGUE ELECTRONICS

Free 1994 Major League Electronics' catalog featuring a full-line of connectors, with a complete range of options on all products. The catalog contains information on Terminal Strip Headers, Socket Strips, Board Stackers, and Shunts/Jumpers.

CIRCLE 200

Major League Electronics

KEPCO SUPPORTS VXI

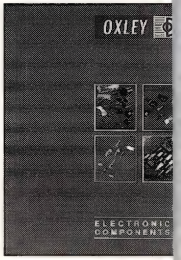
The Kepco model TMA VXI-27 provides a gateway from a XVI card to KEPCO programmable power supplies. Kepco, with the introduction of the model TMA VXI-27, announced support for the VXI bus by providing an interface path to all of the Kepco M-series power supplies.

CIRCLE 201

KEPCO

ELECTRONIC COMPONENT

1994 Catalog contains technical info on our full range of components which include: EMI/TVS Filters, Planar Arrays, Trimmer Capacitors, Led Indicators NVG Displays, Elapsed Time Indicators, Test Points for pcbs, fiber optics.



CIRCLE 202

OXLEY INC.

Device Programming Tools

The Newest Advances are presented in over 20 pages, illustrating the widest selection of development and production tools, PLO/FPGA Design software, UV erasers, and Prom/PLD Programmers from the leading manufacturer.

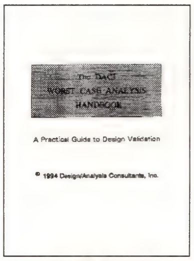
CIRCLE 203

LOGICAL DEVICES, INC.

DESIGN VALIDATION

Use DACI's Handbook to achieve reliable, cost effective, optimized designs, without the need for complex math.

$49/Copy
(Free with purchase
of DACI's worst case
Analyzer software.


The DACI
WORST CASE ANALYSIS
HANDBOOK
A Practical Guide to Design Validation
© 1994 Design/Analysis Consultants, Inc.

CIRCLE 204

Design Analysis Consultants, Inc.

Microcomputer Modules & CA

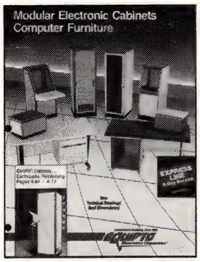
The catalog describes 6800 and 6809 single-board computers, input/output interfaces debuggers, compilers and assemblers; plus schematic capture and printed circuit board layout software and accessories for the IBM personal computer.

CIRCLE 205

Wintek Corporation

Much New In Free Enclosures Catalog

More EMI/RFI shielded cabinets are offered. Shielding effectiveness test data have been revised. Earthquake reinforced enclosures have been added. New, too are dual dimensioned technical drawings in this over 300-page free catalog on modular cabinets, and computer furniture

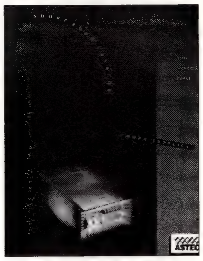


CIRCLE 206

EQUIPTO ELECTRONICS

Free Power Supply Catalog

Astec's new catalog features low power supplies with high efficiency, high power supplies with PFC, distributed power modules and PC supplies meeting new EPA standards call power fax for datasheets by fax 619-439-4266.

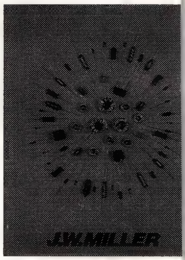


CIRCLE 207

ASTEC STANDARD POWER

INDUCTOR CATALOG

J.W. Miller, Gardena, CA 44-page catalog and coil selector guide covers fixed & adjustable RF coils, toroids, high-current filter chokes, molded & conformal coated chokes, and surface mounted inductors...Values from .01 uH-500,000 uH.

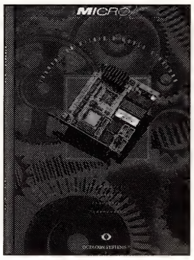


CIRCLE 208

J.W. MILLER

Embedded PC Catalog

Octagon System's, Westminster, CO, 112-page catalog displays their Micro PC® family. The Micro PC line is designed for apps. where small size wide temperature range, and rugged packaging are critical. ISO 9001 certified.



CIRCLE 209

OCTAGON SYSTEMS

DIN CONNECTORS

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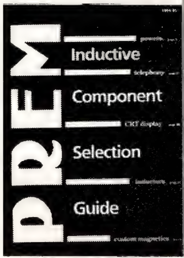

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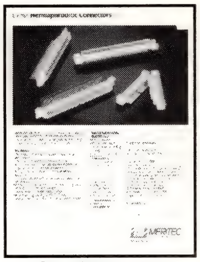

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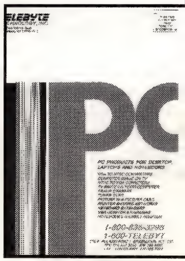

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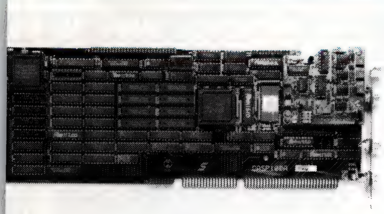

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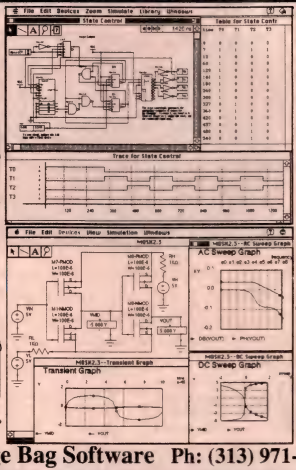

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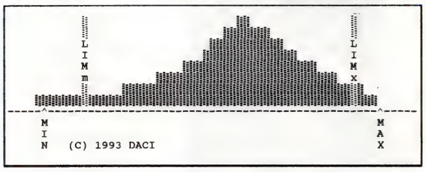

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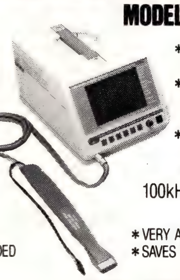

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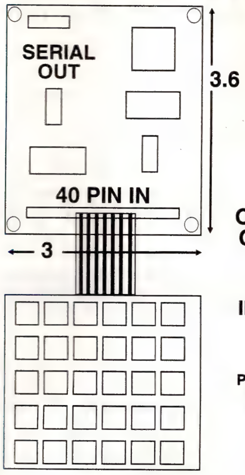

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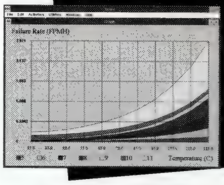

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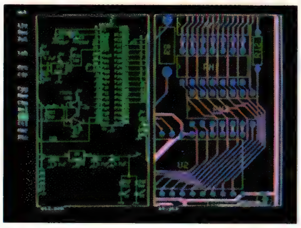

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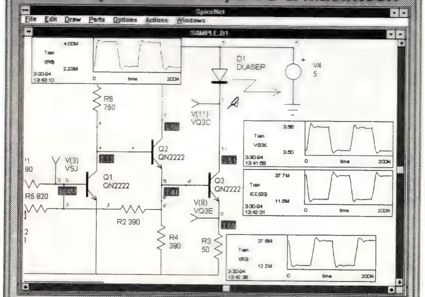

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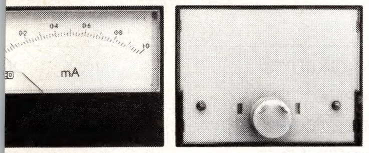

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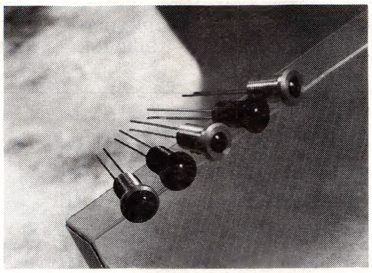

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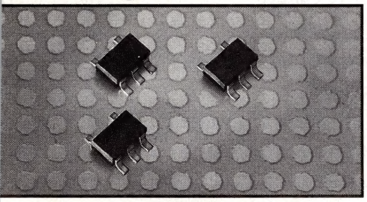

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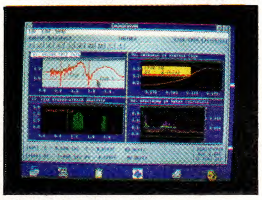

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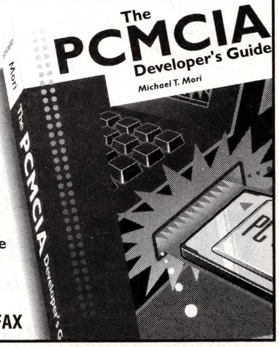

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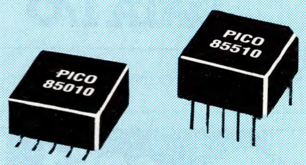

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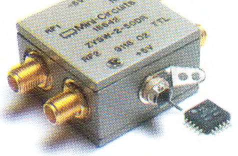

SPECIFICATIONS (typ)	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) $14.95 ZYSW-2-50DR (SMA) 59.95		

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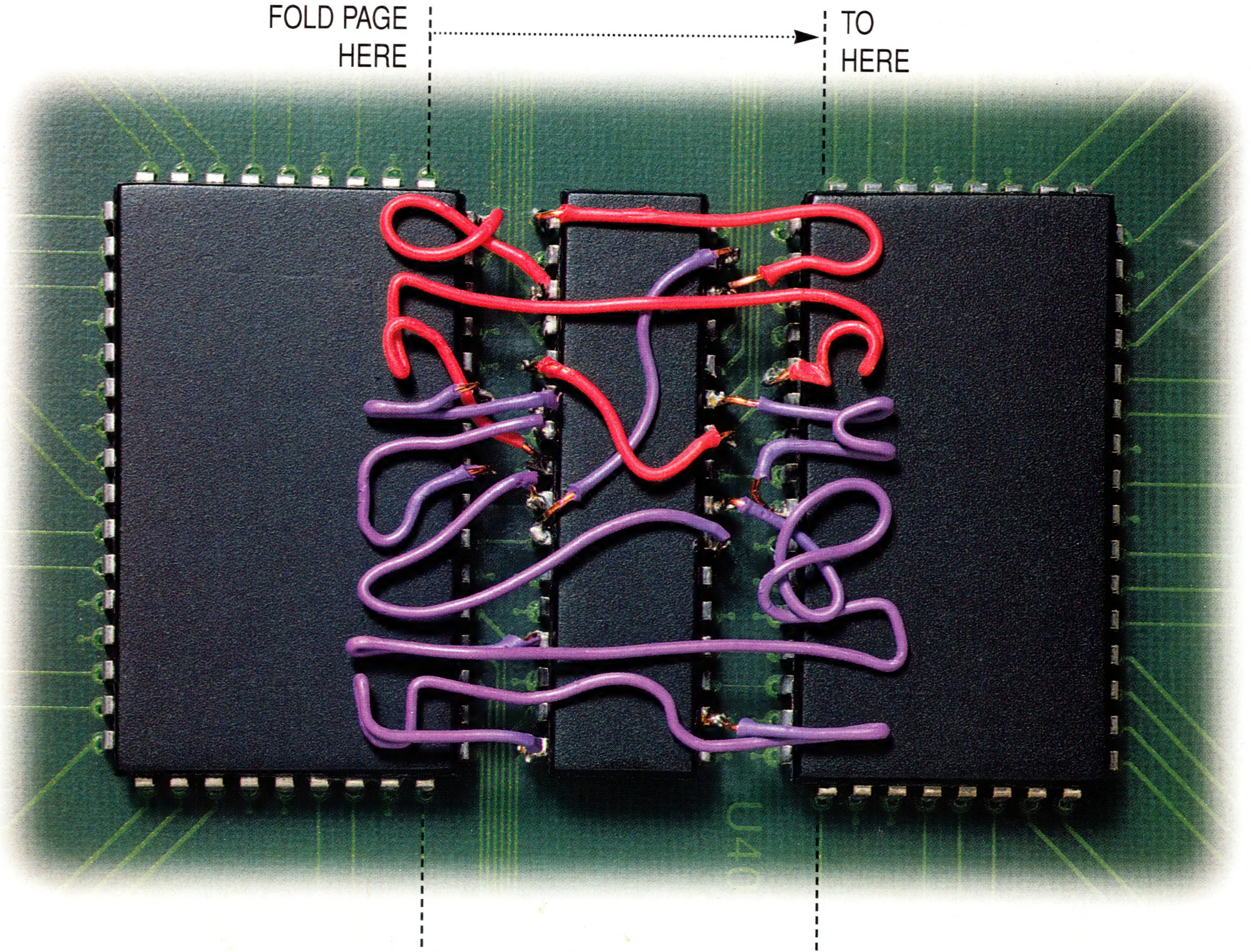

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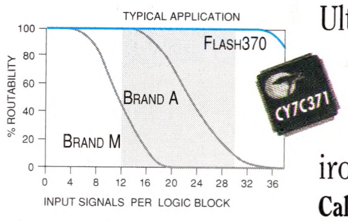

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